Chapter 3

Resistive Switching at Nb-doped SrTiO$_3$ Interfaces

Abstract

In this chapter, we use relatively large Ni contacts on Nb:STO to study the interfacial resistive switching effect. In the first part of this work, the possibility of multi-level switching is demonstrated by gradually sweeping the applied voltage. By changing the magnitude of the reverse bias reset voltage, the devices can be switched to higher resistance states so that multi-level storage can be realised. Based on these results, we discuss the switching mechanism. The reliability of the devices, with respect to retention and endurance, was investigated by performing repeat cycles of resistance switching. Next, we look at how the resistance state can be changed by applying voltage pulses. This is of importance for emulating synaptic behaviour, where resistance changes are brought about by the spiking behaviour of neurons. In the latter part of the chapter, we model the device behaviour with the goal of developing a learning algorithm that could be used for training a network of integrated devices.

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3.1 Introduction

In most ionic material systems where memristive behaviour has been demonstrated, switching is absent in the as-fabricated device and an electroforming process, during which the device is subjected to a high bias, is needed to induce the switching [4–7]. The details of the forming process are well discussed in literature, but pose limitation on the operation of memristors at low powers due to the requirement of the high forming voltage. Additionally, a lack of control over the forming process can increase device-to-device variations and reduce device performance[4, 6, 8, 9]. Interfacial devices have the potential to show less variability and precise analogue tuning of the conductance, but their properties are less widely investigated. There has been a growing interest in understanding the rich and intricate properties of complex oxide interfaces and their application in superconductivity, magnetism and multiferroics [10–13]. The Schottky interface of Nb:STO offers rich electronic properties that have been shown to be useful both for memristor and spintronics applications [14–17]. In particular, interfacial switching has been observed at Schottky interfaces between Nb-doped SrTiO$_3$ (Nb:STO) and metals, without the need for a forming process[7, 18–26].

An important parameter is the non-linear variation of the large dielectric permittivity ($\epsilon_r$) with temperature and electric field, as shown in Fig. 3.1(a) and (b), respectively[27, 28]. The tuning of the potential profile of the conduction band of Nb:STO with electric field and temperature gives rise to charge transport characteristics that are unique and are not observed in conventional semiconductors like Si, GaAs and Ge.

In this chapter, we use relatively large metal contacts on Nb:STO to study resistive switching. The simplistic structure of these pillars lends itself well to downscaling, which is explored in chapter 4. In the first part of this work, the possibility of multi-level switching is demonstrated by gradually sweeping the applied voltage. By changing the magnitude of the reverse bias reset voltage, the devices can be switched to higher resistance states so that multi-level storage can be realised. From this, important information about the resistance-switching mechanisms is also inferred. The second part of this work focused on how the resistance state can be changed by applying voltage pulses. This is of importance for emulating synaptic behaviour, where resistance changes are brought about by the spiking behaviour of neurons. The reliability of the devices, with respect to retention and endurance, was investigated by performing repeat cycles of resistance switching.

To enable computer-aided integrated circuit design of memristors, it is paramount to have reliable models of the devices’ electrical behaviour to enable simulation and prediction of the behaviour of both individual memristors as well as of the whole integrated circuit. Consequently, substantial effort has gone into developing models
for filamentary switching, simulation models for interfacial switching, however, are not widely available\cite{29}. This is investigated in section 3.7. To start this chapter, we will review the literature on Nb:STO resistive switching in section 3.2.

![Image](https://via.placeholder.com/150)

**Figure 3.1: Dielectric permittivity of STO:** as a function of (a) temperature (reprinted with permission from \cite{27}) and (b) electric field.

### 3.2 Literature on Resistive Switching in Nb:STO

It is often postulated that a layer close to the interface layer is responsible for the switching \cite{18,30,31}. This has been verified by capacitance-voltage measurements where this layer provides a parasitic interfacial capacitance, resulting in an additional voltage drop. Some groups have shown that both high and low resistance states show an area-independent current density, eluding to a switching mechanism that occurs homogeneously over the entire device area \cite{32}. In this case, switching occurs through a change in the amount of trapped charge in the interfacial layer towards a more positive value in the low resistance state (LRS) and a more negative value in the high resistance state (HRS). This can occur through charge trapping and detrapping at the interface \cite{18,20,26,30,33} and/or movement of oxygen vacancies \cite{20,33}, which affect the Schottky barrier height and width.

Recently it was suggested that moisture trapped at the interface plays an important role in the switching process. Grain boundaries in the metal electrodes and
defects at the surface of Nb:STO provide sites where water molecules can be captured. This can serve as a source of protons which assist electron trapping and barrier height modulation. Kunwar et al. found that when protons are removed from the interface the current-voltage hysteresis is significantly reduced, but can be restored by reintroducing moisture[34].

It has also been proposed that the application of a positive bias results in the generation of oxygen vacancies, forming tunnelling paths and giving rise to an LRS where tunnelling, rather than thermionic emission dominates charge transport. The application of a negative bias results in the accumulation of large amounts of oxygen in the vacancies which prevents tunnelling and gives a HRS [35, 36].

Other explanations are proposed where the barrier profile is unchanged and interfacial changes happen in local regions. Rodenbuecher et al. used local-conductivity AFM on highly doped Nb:STO to show the presence of nanoscale conducting and switchable clusters. Suggesting that in this case switching is a local phenomenon related to the presence of conducting clusters with higher Nb content than their surroundings [37].

D. S. Shang et al. suggested that the overall Schottky barrier height does not change, but instead, there are small active regions with transport properties sensitive to external fields at the interface. They act as faucets that can be opened or closed by electrical pulses, acting as a circuit consisting of a diode and a resistor in parallel. A positive voltage pulse depresses the resistor but has little effect on the diode, causing the high-to-low resistive transition. The total area of the active region could be substantially smaller than that of the interface[38].

D. Kan et al. observed no clear area dependence of the current, suggesting an inhomogeneous current flow across the interface and that the current conduction area is smaller than the size of the top electrode. The capacitance was found to linearly increase with increasing electrode area for both resistance states, suggesting that the same depletion layer exists in the overall junction. This is also indicative of the existence of the local conducting paths instead of a homogeneous current flow and can be explained by the existence of local conduction channels across the interface and that the current flows along the channels for both resistance states. The difference between HRS and LRS is brought about only by the conducting channels. They found the as-fabricated junctions to be close to an LRS, suggesting that the local conduction channels intrinsically exist in the Nb:STO crystals and that inhomogeneity in chemical composition or defects near the interface could be the origin of the channels[39].

Y. L. Chen et al. used scanning tunnelling microscopy and spectroscopy to study the resistive switching in Nb-doped SrTiO$_3$ without an electrode. They demonstrated that oxygen migration is the dominant mechanism for the variation of the electronic structure during the switching. With a negative voltage, oxygen anions at the interface near the STM tip were oxidised into oxygen molecules and left the
lattice. Simultaneously, oxygen vacancies diffuse into the sample, which act like donor-like levels causing distortions in the local density of states (LDOS) near the conduction band, enhancing the carrier concentration with electron hopping, resulting in an increase in conduction. With a positive voltage, oxygen anions return into the sample, reducing the influence of the donor-like level and decreasing the conductivity\[40\].

Despite a large number of contradictory results and explanations, factors of importance that have been identified include the semiconductor doping concentration, electrode material and the quality of the interface.

Because Nb:STO is an n-type semiconductor with a work function of 3.9 eV, the barrier formed when interfaced with low work function metals, such as Ti or Al will be low, allowing for Ohmic behaviour. In this case, no resistive switching is observed\[18, 20, 41, 42\]. The work function of the metal electrode should be sufficiently large to form a Scottky barrier for switching to occur.

Hysteretic current-voltage behaviour is not observed when the doping concentration is too high. This could be because with increasing doping Nb:STO quickly becomes a degenerate semiconductor and both the effective barrier height and built-in potential are reduced with increasing Nb concentration, which may result in an Ohmic-like contact between metal and Nb:STO\[23\]. It has also been proposed that with increasing doping, the barrier width is reduced leading to an increase in tunnelling and an excess current\[35\].

Mikheev et al. demonstrated the resistance ratio in Pt/Nb:STO is governed by the quality of the interface. When high-quality epitaxial Pt contact with almost no interfacial defects almost no hysteresis was observed. The typical deposition techniques used to fabricate metal contacts are at room temperature and give rise to polycrystalline contacts which can result in interfacial defect layers found to be important for modulating charge trapping and detrapping, highlighted by an increasing resistance ratio with decreasing interface quality\[18\]. They further exploited this by intentionally introducing interfacial defects by inserting non-stoichiometric, SrTiO\(_3\) layers between the metal/Nb:STO. They found that these interlayers significantly change the switching behaviour and increase state retention\[43\]. It should, however, be noted that resistive switching has been observed with SrRuO\(_3\) as the electrode material. In this case, the metal can be deposited epitaxially at elevated temperatures using pulsed laser deposition resulting in a highly crystalline film and a clean interface\[35, 44, 45\]. Kunwar et al. also studied the effect of interface quality by annealing Nb:STO substrates at different temperatures. Annealing increases the interface quality by reducing surface dangling bonds and vacancy defects as well as removing carbon and other organic molecules. They found that the resistance ratio decreases as the annealing temperature increases. The quality of the top electrode, however, was determined to have a stronger effect on the ratio than the Nb:STO
3.3. Experimental Details

Here relatively large structures for Ni contact pillars (100 × 200 μm²) on Nb:STO are used; the simplistic structure of these pillars lends itself well to down-scaling. Devices were fabricated on n-type doped (001) SrTiO₃ single crystalline substrates with 0.01 wt% Nb doping, obtained from Crystec GmbH. To remove the SrO sublattice from the top surface and obtain TiO₂ termination the substrates were treated with buffered hydrofluoric acid and deionised water. This was followed by the immediate deposition of 20 nm of Ni, capped with 20 nm of Au by electron beam evaporation at a base pressure of 10⁻⁶ Torr. Three terminal (3T) geometry meso-structures were

surface quality[34].

Figure 3.2: Temperature dependent device characteristics. (a) Three terminal (3T) device geometry where a voltage (V_Dc) is sourced between central contact 2 and a grounded reference contact 1, giving rise to a potential drop between contact 2 and reference contact 3. The measurement scheme used is 4-probe and the junction voltage (resistance R_int) is measured, decoupled from the resistances due to the leads and the semiconductor channel (R_wf). (b) Potential profiles for different polarities of V_Dc: positive (forward bias) and negative (reverse bias) across the Schottky interface of Nb:STO with Ni at room temperature. (c) Temperature-dependent I-V characteristics for a contact (100 × 200 μm²) where the current is plotted with junction voltage. (d) Increase in the reverse bias current on decreasing temperature, as shown by the crossover of the reverse current between 75 K and 300 K. The potential profile shows narrowing of the conduction band in STO at 75 K resulting in increasing current due to enhanced tunnelling.
3. Resistive Switching at Nb-doped SrTiO$_3$ Interfaces

Figure 3.3: Room temperature dependent device behaviour. (a) I-V characteristics of the device obtained by performing repeat cycles in which the voltage was swept between $+1$ V and a varying $(-1$ V (black), $-2$ V (red), $-3$ V (blue) and $-4$ V (purple)) reverse bias voltage. Each subsequent cycle was done after a delay time of 300 s at $+1$ V. The upper branch of each cycle is the low resistance state (LRS) and the lower branches are the high resistance states (HRSs). (b) Resistances calculated from the cycles performed in (a); the lower branches are the trace directions and the upper branches are the retrace directions. (c) Ratios of the HRS (lower branch) and LRS (upper branch) resistance values calculated from (a).

fabricated by UV lithography and Ar-ion etching. This device geometry is shown in Fig. 3.2(a).

In order to investigate the Schottky contact of Ni on Nb:STO, current-voltage (I-V) measurements were performed in a 4-probe, three-terminal (3T) geometry using a Keithley 2410. In this geometry, a dc-voltage ($V_{DC}$) is sourced between a central
contact 2 and a grounded reference contact 1 (shown in Fig. 3.2(a)), giving rise to a potential drop between contact 2 and reference contact. The current is measured between contact 2 and source contact 1. This geometry ensures that the potential drop \( V \) is caused solely by the interface resistance \( R_{int} \) of contact 2 and eliminates series resistances from the leads, semiconducting channel \( R_{wf} \) and the two reference contacts. Isolating the effect of a single Schottky interface gives a better understanding of the transport mechanisms that are controlled by the electric field across the interface with Nb:STO.

3.4 Results

The temperature-dependent I-V characteristics of a junction of 100 \( \times \) 200 \( \mu \)m\(^2\) are shown in Fig. 3.2(c). At each temperature, the current is plotted with respect to \( V \), following a sweep from 0 V \( \rightarrow \) +1 V \( \rightarrow \) 0 V \( \rightarrow \) -2 V \( \rightarrow \) 0 V. The I-V characteristics clearly show the existence of a Schottky barrier at the Ni/Nb:STO interface. Transport in forward bias is governed by thermionic emission. Upon increasing the voltage, the conduction band of Nb:STO is raised with respect to the Fermi level \( E_F \) of Ni, as shown in Fig. 3.2(b), resulting in a decrease in the width of the depletion region and the built-in electric field. At low temperatures, there is less thermal energy available for electrons to overcome the barrier and consequently, larger voltages are required for transport compared to higher temperatures. Current density, \( J \), can be described by Eq. 2.7.

In reverse bias (negative \( V_{DC} \)), a strong response of the dielectric permittivity of STO \( (\epsilon_r) \) to the increasing built-in electric field results in a steeper bending of the conduction band of STO as shown in Fig. 3.2(b). This decrease in the effective barrier width at \( E_F \) promotes tunnelling, allowing current to flow in the reverse bias regime. The reverse current increases upon lowering the temperature as illustrated in Fig. 3.2(d) where 75 K and 300 K are compared. Upon reducing the temperature, \( \epsilon_r \) increases and becomes more sensitive to electric fields, resulting in a significant narrowing of the conduction band potential and allowing for enhanced tunnelling \[46, 47\]. In summary, the charge transport is governed by thermionic emission of charge carriers in the forward bias regime and by temperature-independent field emission in reverse bias.

The reverse bias hysteretic response of the resistance embodies the colossal electroresistance (CER) effect. The Schottky interface of Nb:STO is replete with trapped charge states in the form of oxygen vacancies that occupy energy levels about 0.5 to 1 eV below the conduction band \[48, 50\]. Their accessibility to electrons flowing into the conduction band in Nb:STO is enhanced by the increasing electric field, giving
3. Resistive Switching at Nb-doped SrTiO$_3$ Interfaces

Figure 3.4: Endurance characteristics of the device over 100 cycles subsequent switching cycles. The First (blue) to 99$^{th}$ cycle was performed following a sequence where, after a 120 s wait time at +1 V, the voltage was swept from +1 V to -4 V and back to +1 V. The black lines show cycles 2-99. Cycle 100 (red) was obtained after a 1 hour set time at +1 V.

rise to the CER effect. This switching is bipolar: the resistance will increase in reverse bias and decrease in forward bias.

Firstly, we investigate using gradual voltage sweeps to study the switching as this provides us with the most transparent insight at every point of a switching cycle. To demonstrate multi-level resistance switching, the bias voltage was swept from +1 V $\rightarrow -V_{\text{reset}} \rightarrow +1$ V. The set voltage (+1 V) and time (300 s), to switch to a low resistance state (LRS), was kept constant while the reset voltage ($V_{\text{reset}}$) was varied (-1 V, -2 V, -3 V and -4 V) to reset to different high resistance states (HRSs). The results of this are shown in Fig. 3.3(a) and illustrate that by changing the reset voltage, states of increasingly higher resistance can be attained. The resistance values corresponding to every part of the loops are explicitly plotted in Fig. 3.3(b). The resistance of the LRS does not change significantly by changing the bias, while the resistance of the HRS peaks at a low bias value and thereafter decreases until reaching the resistance value of the LRS at the maximum reset voltage. This is mimicked in Fig. 3.3(c), where the ratio of the resistance of the HRS over the LRS is extracted at every reverse bias value.

We investigated the room temperature endurance and cycle-to-cycle resistance variations by performing 100 subsequent cycles between +1 V and -4 V and back, shown in Fig. 3.4. The first 99 cycles were done with a set time of 120 s at +1 V between cycles. The last cycle was performed after a 1-hour set time at +1 V. There
3.5 State retention

Next, we focus on how the resistance state can be changed by applying voltage pulses. This is of importance for emulating low-power synaptic behaviour, where resistance changes are brought about by the spiking behaviour of neurons [21]. The retention of the LRS and HRS was investigated by setting the respective states in two ways. Firstly, by the voltage sequence shown in the bottom panel of Fig. 3.5(a): here the LRS was set by sweeping $0 \text{ V} \rightarrow +1 \text{ V} \rightarrow 0 \text{ V}$ with a set time of 120 s at $+1 \text{ V}$. This was followed by a negative bias read pulse of $-1 \text{ V}$. The device was subsequently set to a HRS by sweeping $0 \text{ V} \rightarrow -4 \text{ V} \rightarrow 0 \text{ V}$ and another read pulse was applied. Secondly, the LRS and HRS were set by applying short pulses of 0.9 s of $+1 \text{ V}$ and $-4 \text{ V}$ respectively, depicted in Fig. 3.5(b). In both cases, the sequences were repeated five times.

The two sets of results demonstrate that the resistance of the HRS does not significantly change either over time or between cycles. The differences in the LRSs resulting from the two setting methods on the other hand, clearly show deviations. When a short pulse is used to set the LRS, the resulting resistance difference between the LRS and HRS is smaller than when a longer pulse is used to set this state. Over time, the resistance of the LRS becomes higher and for the short pulse setting method the
3. Resistive Switching at Nb-doped SrTiO$_3$ Interfaces

High and low resistance states reach similar resistance values more rapidly.

3.6 Switching Mechanism and Discussion

Stable bipolar resistive switching was present in the as-fabricated device without a required electroforming process. This indicates that the nature of the switching is not mediated by the formation of local filamentary paths, as is seen in many oxides that are initially insulating. The Schottky nature of the transport characteristics is evident from the temperature dependence of the charge-transport measurements shown in Fig. 3.2(c). The importance of the existence of the Schottky barrier in realising switching is evident from junctions where no proper Schottky contact was established which do not exhibit hysteresis. Both these observations confirm the interfacial origin of the resistive switching [20–23].

Estimations of the barrier heights in the LRS and HRS, realised using a set voltage of +1 V and a reset voltage of -4 V, were made by fitting Eq. 2.7 in the forward bias regime. This gives a value of 0.72±0.01 eV for the LRS and 0.76±0.01 eV for the HRS. The height of the barrier is smaller in the LRS than in the HRS, allowing for an increase in the number of electrons able to overcome the barrier in the forward bias regime, where charge transport is governed by thermionic emission (see Fig. 3.2(b)).

Resistive switching is the result of a change in the charge at the interface from a more negative to a more positive value between the HRS and LRS. In literature, both the redistribution of oxygen vacancies and the trapping and de-trapping of electrons at the interface under electric fields have been linked to this change [18, 21, 23, 31]. After switching, it is observed that both the LRS and HRS asymptotically approach a stable value over time: the resistance of the LRS becomes higher, while the resistance of the HRS becomes lower. In both cases, the resistance $R$ over time $t$ could be fit using the Curie-von Schweidler equation $R \propto t^n$ [18] with rate-related exponents, $n$, for the LRS and HRS of 0.685 and -0.244 respectively (see Fig. 3.6). This change is associated with capacitive charging and is typically observed in high-$\kappa$ materials due to the trapping of charges under bias [18, 20, 21, 26].

Under the influence of a reverse bias voltage, the mobile electrons are trapped at defects and oxygen vacancy sites which results in a reduction in the positive charge at the interface. Consequently, the barrier becomes higher and wider resulting in a switch to the HRS. When electrons become de-trapped from the interface, the charge in this region becomes more positive, resulting in a reduction of the height and width of the Schottky barrier giving the LRS. When switching from the HRS to LRS, charges are de-trapped, and more trap states are available at the interface. Over time, negative charges will again become trapped in these states resulting in a progressive increase in the resistance of the LRS. Fig. 3.3(a) shows that the hysteresis in the for-
3.6. Switching Mechanism and Discussion

Figure 3.6: Fits (shown in red) of the Curie-von Schweidler equation to LRS and HRS after setting the respective states with voltage sweeps between 0 V and +1 V and -4 V. The extrapolation of these fits was used to estimate the retention time.

ward bias direction (governed by thermionic emission) is less significant than in the reverse direction (governed by tunnelling) which suggests that the resistive switching does not originate purely from changes in the profile of the barrier. Trap-assisted tunnelling may also contribute to transport and when the trap states become filled, these paths become blocked so that tunnelling is suppressed \[31\]. When the magnitude of the reverse bias reset voltage is increased, the magnitude of the electric field across the interface increases and electrons going from the metal to the semiconductor side tunnel from states further below the Fermi level. Consequently, a larger range of interfacial states is available in which they can be trapped, resulting in an increase in the resistance of the HRS obtained upon increasing the reset voltage.

Fig. 3.5 demonstrates that there is almost no variation in the HRS after repeat cycles, and there is no difference in the value realised by the sweeps and pulses. The LRS state, on the other hand, is affected more significantly and the resistance achieved with a longer setting process is noticeably lower and reproducible upon cycling. These observations are in accordance with the increasing resistance of the LRS upon cycling (Fig. 3.4) and indicate that the setting process is slower than resetting. While within the time the states were monitored, the difference in the resistance states remained substantial, the progressive change of the LRS (HRS) towards a state of higher (lower) resistance could indicate that over time both will tend to a steady state of intermediate resistance. By extrapolating the Curie-von Schweidler fits from Fig. 3.6 an estimate of 12,400 s (~ 3.5 hours) is obtained for this retention time. A
similar analysis was done for the measurement performed using pulses to set the states and here a retention time of 4150 s (∼1 hour) is estimated. This kind of relaxation is typically observed in systems where the switching mechanism is related to charge trapping and de-trapping [31].

Fig. 3.5 eludes to a temporal dependence on the setting process to realise the LRS. The two different methods for setting the LRS can be used to mimic learning and forgetting in short-term memory: when a relatively long stimulus (a positive bias voltage) is used to set the device to a state of low resistance and the resistance is monitored immediately after, there is a significant decrease in resistance with respect to before the stimulus. Over time, this state will approach a state more similar to before the stimulus [9, 21]. If, on the other hand, a shorter pulse is used to set the LRS, the state of the device is less significantly affected. Like before, directly after presenting the stimulus the resistance state will be lowest, but in this case, the device will tend to a state reminiscent of its state before the stimulus considerably faster. This can be compared to the fading of memory as time passes: less significant events (in this case, a shorter pulse) will be forgotten faster.

From Fig. 3.3(a) it is clear that multi-level switching can readily be achieved by changing the magnitude of the reset voltage. In this way, a plethora of resistance states can be defined at a single low bias read voltage. The gradual, rather than abrupt, nature of the resistance change not only mimics the analogue nature of synapses but also allows for large storage. The small amount of current flowing in the reverse bias regime gives rise to large resistance values (plotted in Fig. 3.3(b)) both in the LRS (∼10^5 Ω) and in the HRSs (up to ∼10^8 Ω). In addition to high resistance values, the resistance ratios between the HRS and LRS are also large (see Fig. 3.3(c)): using -1 V as a read voltage, a maximum ratio of ∼10^3 can be obtained.

3.7 Modelling

Large-scale integration of memristors will require computer-aided circuit design. To achieve this, it is important to have reliable models of the devices’ electrical behaviour, enabling simulation and prediction of the behaviour of both individual memristors as well as of a whole circuit. In addition, such models will aid in the development of learning algorithms for training memristive networks.

3.7.1 Hysteretic Behaviour*

Figure 3.7(a) shows the resistances of HRSs shown in Fig. 3.2 as a function of the applied voltage, V after sweeping to different reset voltages, \( V_{\text{reset}} \). It can be seen

*Model developed by L. R. B. Schomaker
3.7. Modelling

Figure 3.7: Modelling hysteretic Behaviour. (a) Resistance in the HRS after switching from reset voltages of -1 V (black), -2 V (red), -3 V (blue) and -4 V (green). Open circles indicate the measured data and the lines are the fits using Equation 3.1. The dependencies of the model parameters found from the fits in panel (a) as a function of the reset voltage are shown in panels (b)-(d), i.e., parameters \( r \), \( b \) and \( f \), respectively. Panel (e) summarises the found constants \( c \) and \( d \). Panel (f): Resistance values on the intermediate reset voltage values (-1.5 V, -2.5 V and -3.5 V). Open circles represent measured data whereas the lines show the model’s predictions.

that in each case the highest resistance is found at a negative voltage close to zero and with increasing \( V_{\text{reset}} \) both the magnitude of the peak resistance and the corresponding voltage increase in magnitude. To describe this, we developed a phenomenological model and found this variation to be well-described by the product of a Gaussian distribution and a Fermi-Dirac-like logistic function:

\[
R(V) = re^{(bV^2+cV)} \times \frac{1}{1 + e^{(d(V+f))}} = \frac{re^{(bV^2+cV)}}{1 + e^{(d(V+f))}}
\]  

(3.1)

We initially assume that the five variables in the equation:
r: Peak resistance.
b: Width of Gaussian distribution.
c: Offset of Gaussian distribution.
d: Steepness of logistic.
f: Horizontal offset of barrier.

can vary as a function of $V_{\text{reset}}$, and a Monte Carlo search is done using the data in Fig. 3.7(a) to determine their values from the fits (solid lines). From this, it is found that the values of $c$ and $d$ are approximately constant and they are taken to constants. Using Monte Carlo optimisation, we find that both $r$ and $b$ have an exponential dependence on $V_{\text{reset}}$, while a linear dependence is found for $f$. These values are summarised in Fig. 3.7(b)-(e). The code is available at Ref. [51].

To assess the model’s predictive power, it was tested on intermediate $V_{\text{reset}}$ values of -1.5 V, -2.5 V and -3.5 V as shown in Fig. 3.7(f), where the experimental data is shown in open circles and the model’s prediction is shown as solid lines. The model agrees well with the experimental data for the higher values and correctly predicts the maximum resistance, the voltage at which it occurs and follows the rest of the sweep reasonably closely for -2.5 V and -3.5 V. The model deviates more significantly for the $V_{\text{reset}}$=-1.5 V sweep and predicts a considerably lower resistance throughout the sweep than what is experimentally observed. This could indicate that when $V_{\text{reset}}$=-1 V, a substantially smaller change in resistance is given than for higher $V_{\text{reset}}$ magnitudes ($|V_{\text{reset}}| >\sim 1.5$ V), leading to difficulties in predicting the low $V_{\text{reset}}$ behaviour. This also indicates that the influence of low reading voltages on the resistance is small.

While this model described the experimental data at each point of the hysteresis loop reasonably accurately and has some predictive power, it is purely phenomenological, limiting its applicability. A more extensive model should consider the physical mechanisms underlying transport, the switching mechanism and the role of the applied field in modulating these factors. We have done this by adapting the Yakopcic model[52] to include transport phenomena relevant to interfacial memristors: this work is presented in Ref. [3].

3.7.2 Weight Update Using Pulses†

Biological synapses strengthen and weaken over time in response to applied stimuli, known as synaptic plasticity, which is thought to be one of the most important underlying mechanisms enabling learning and memory in the brain. For a device to be

†Work in collaboration with T. F. Tiotto, J. P. Borst and N. A. Taatgen
3.7. Modelling

Figure 3.8: Device response to pulses. (a) Device response to the application of multiple RESET pulses of -4 V. (b) Device response to the application of multiple SET pulses of varying amplitudes of +0.1 V (black), +0.5 V (blue), and +1 V (red). 10 RESET pulses of -4 V are applied to increase the resistance before the application of the potentiation pulses.

useful as a synaptic component, its resistance should thus be controllable through an external parameter, such as voltage pulses, so that it may take on a range of values (within a certain window).

To investigate the accumulative effect of applying pulses across the interface, we conducted a series of measurements in which a device was subjected to a set voltage of +1 V for 120 s to bring it to a low resistance state and reduce the influence of previous measurements. Then, 25 reset pulses of negative polarity were applied and the current was read after each pulse. A negative read voltage was chosen because significantly larger hysteresis is observed in reverse bias compared to forward bias. Because of differences in the charge transport mechanisms under forward and reverse bias, a significantly lower current flows in this regime: to ensure the measured current is sufficiently large to be read without significant noise levels, a reading voltage of -1 V was chosen. The reset pulse amplitude was varied from -2 to -4 V. This procedure was repeated several times for each amplitude sequentially. The pulse widths were ~1 s.

Next, we performed a set of measurements in which devices were set to a low resistance state by applying +1 V for 120 s before applying 10 reset pulses of -4 V to bring devices to a depressed state. This was followed by applying a series of potentiation pulses ranging from +0.1 V to +1 V.

We investigated the effect of applying pulses across the interface by administering a long set pulse followed by 25 reset pulses. Due to the resistance’s dependence on the memristor’s history, there is some variation in the starting state, shown by the measurement at pulse number 0. Figure 3.8(a) shows the results for pulses of -4 V in amplitude. The first pulse gave rise to the largest increase in resistance, with
subsequent ones having a considerably smaller effect.

The change in resistance quickly levelled off and the influence of subsequent pulses was significantly smaller. The application of a reset pulse resulted in a switch to a high resistance state that depended strongly on the amplitude of the applied pulse, but not strongly on the number of pulses of that amplitude that were applied.

We also explored the devices’ response to set pulses. It should be pointed out that in Fig. 3.8(b) the initial state (and hence also the large difference induced by the first reset pulse) after applying a long set voltage, which would correspond to pulse number 0, is not shown. Note that different pulse amplitudes were chosen for set and reset pulses because the asymmetric nature of the charge transport results in substantially larger currents in forward bias (Fig. 3.3). With the application of positive pulses, the device saw its resistance gradually decrease (potentiation). It is clear that in this case both the pulse amplitude and the number of applied pulses had a great impact on the resistance state of the device. The larger the amplitude of the set pulse, the greater the induced difference to the resistance with each applied pulse. Interestingly, compared to applying reset pulses, the difference between the change induced by the first and later pulses was not severe. While 10 applied reset pulses gave rise to close to saturated high resistance states, this was not observed when positive pulses were applied.

![Figure 3.9: Power law.](image)

(a) Circles show the experimental data of device resistance after the application of multiple SET pulses with amplitudes varying from +0.1 V (top branch) to +1 V (bottom branch). Lines represent fits to Eq. 3.2. (b) Black circles show the exponents extracted from the fits in (a) as a function of pulse voltage. The red line is a linear regression fit from which the a and b parameters are obtained.

To model their behaviour in response to set pulses on the basis of the experimental measurements we carried out. The device behaviour when applying a series of
set pulses, was seen to be well-described by an exponential equation of the form:

$$R(n, V) = R_0 + R_1 n^{a+bV}$$  \hspace{1cm} (3.2)

in which $V$ represented the amplitude of the set pulse, $n$ the pulse number, $R_0$ the lowest value that the resistance $R(n, V)$ could reach, and $R_0 + R_1$ the highest value. One of the reasons we chose a fit of this form was because of the parallel we saw with the classic power law of practice, a psychological and biological phenomenon by virtue of which improvements are quick at the beginning but become slower with practice. In particular, skill acquisition has classically been thought to follow a power law [53, 54].

By solving Eq. 3.2 for $n$, we can calculate the pulse number from the current resistance $R(n, V)$ by:

$$n = \left( \frac{R(n, V) - R_0}{R_1} \right)^{\frac{1}{a+bV}}$$  \hspace{1cm} (3.3)

Parameters $a$ and $b$ were found based on the data measured by applying set voltages between $+0.1$ V and $+1$ V to the memristive devices, as shown in Fig. 3.9(a). The exponents of the curves best describing the memristors’ behaviour were then fitted with linear regression on the log-transformed pulse numbers and resistances, shown in Fig. 3.9(b), in order to obtain a linear expression $a + bV$. This process yielded an estimated best fit for the memristor behaviour of:

$$R(n, V) = 200 + 2.3 \times 10^8 n^{-0.093-0.53V}$$  \hspace{1cm} (3.4)

Discussion

![Figure 3.10: Characteristics defining weight update](image)

Figure 3.10: **Characteristics defining weight update:** (a) dynamic range, (b) linearity and (c) symmetry. The first half of the x-axis is the potentiation regime and the second half is the depression regime. The arrow indicates the direction of increase of each parameter. Inspired by [55].

The dynamic range (on/off ratio or memory window) is the range of values the weight can take on between the HRS and LRS (Fig. 3.10(a)). A larger range tends to
be favourable for higher accuracy\cite{33}. The concepts of linearity and symmetry refer to the relationship between the conductance change and the weight-update pulse number or voltage polarity. Linearity refers to the degree of curvature of the weight update: if the weight update is linear, the conductance change is independent of the pulse number while for nonlinear updates typically the change in conductance decreases with increasing pulse number as shown in Fig. 3.10(b). Symmetry refers to how the difference between potentiation (conductance increase) and depression (conductance decrease), as demonstrated in Fig. 3.10(c).

There is a significant debate in the literature regarding the ideal weight update of experimental devices with respect to linear/non-linear and symmetric/asymmetric characteristics\cite{29,56,57}. It is often argued that ideal devices show linear and symmetric behaviour as inconsistent conductance changes make it more difficult to tune the conductance to a particular value with identical pulses, resulting in training accuracy loss\cite{55}. Of the two, symmetry has been shown to be more important for achieving high accuracy, and it was demonstrated that good accuracy is possible with high symmetry and relatively large nonlinearity\cite{58–60}. Many works have demonstrated that neuromorphic hardware implementing back-propagation for training show higher accuracy with linear weight updates\cite{61–64}. It has, however, been demonstrated that this does not hold for training spiking neural networks (SNNs) where non-linear synapses enable better performance\cite{57,65,66}.

Fig. 3.3 shows that the devices investigated here have a large dynamic range (~ three orders of magnitude), which is favourable for accuracy. We will discuss how this range can be further increased by reducing the device dimensions (chapter 4) or by increasing the doping concentration (chapter 5). Utilising the power-law in Eq. 3.4 as a learning algorithm in an SNN, we have shown that high accuracy can be achieved in approximating universal functions, the main function of machine learning\cite{2}. This highlights the suitability of nonlinear characteristics for training SNNs. At this stage, however, we have largely ignored the depression regime (Fig. 3.8(a)) and we find a large degree of asymmetry. The effect of negative pulses is seen to be significantly stronger than positive pulses. This can be mitigated by reducing the pulse time and amplitude as shown in Appendix A.

### 3.8 Conclusions

Bipolar resistive switching at the Schottky interface of Ni and Nb-doped SrTiO$_3$ was investigated. Measurements were conducted to specifically address characteristics important for neuromorphic computing, including endurance upon repeat cycles, retention, power consumption, and multilevel switching. By changing the reset voltage, multi-level switching was demonstrated between highly resistive states with re-
sistance variations up to three orders of magnitude. The resistive switching showed no permanent degradation during a sequence of 100 switching cycles and showed no signs of fatigue over subsequent measurements. Time was identified as an important parameter governing the setting of the LRS. The retention time of the LRS was seen to increase upon increasing the time of a presented voltage stimulus in a fashion similar to the processes of learning and forgetting in the human brain. Upon the application of voltage pulses, the resistance changes in an incremental fashion - this can be well described by a power law.
3. Resistive Switching at Nb-doped SrTiO$_3$ Interfaces

References


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