Chapter 1

Introduction

1.1 Neuromorphic Computing

Figure 1.1: Computing architectures. (a) Development of microprocessors over time. Graphs plotted using data from [1]. (b) The von Neumann architecture: the memory and processing units share a common bus, giving rise to a memory bottleneck. (c) Brain-like architecture: memory and processing units and co-located. Inspired by [2].

The earliest examples of computers were simple instruments made up of mechanical components, such as the abacus in ancient times. In the mid-1900s electrical components became widely used; these have the advantage that, unlike mechanical components, they are readily reconfigurable and hence can be used for a wider range of applications. The invention of transistors in 1947 further revolutionised computers as they are smaller than the previously used components and consequently could be used to build dense arrays. At the same time the develop-
1.1. Neuromorphic Computing

The advent of semiconductors such as silicon allowed for the integration of large arrays on chips so that large amounts of computing power could be placed in a relatively small area.

This was the beginning of Moore’s law; the continuous shrinking of electronic components to increase the packing density and improve the performance of computing chips. Since the 1970s the number of transistors has approximately doubled every two years and the transistor size has decreased from $\sim 10 \mu m$ to $\sim 1$ nm. Clock frequencies plateaued around 2005, as can be seen in Fig. 1.1(a), and since then there has been a growing memory wall; the speed of processing units exceeds that of the memory units and consequently, data cannot be provided fast enough and processors are held up waiting for memory[4, 5]. This issue is often referred to as the von Neumann bottleneck and is illustrated in Fig. 1.1(b). Simultaneously there are fundamental scaling limits as component sizes are approaching the atomic scale and smaller electronic components are prone to thermal noise and leakage via tunnelling.

Further advancements in computing should not only focus on increasing packing density but also on integrating more functional intelligent components on chips[5]. Hence, developing smart materials and devices, and integrating them into novel architectures that effectively use their properties is the key to beyond von Neumann computing. In this respect, neuromorphic (or bio-inspired/brain-like) computing approaches are a leading candidate due to the remarkably low operation energy and high information processing efficiency of biological systems. This efficiency, both in terms of speed and energy, stems largely from the use of massively parallel networks present in these systems. The human brain consists of $\sim 10^{11}$ neurons[7], connected through $\sim 10^{14}$–$15$ synapses[8]; these units are organised in a three-dimensional network so that there is no separation between the components that perform memory and processing (Fig. 1.1(c)).

Artificial neural networks (ANNs) based on software have enabled a vast range of cognitive applications. ANNs use a collection of nodes called artificial neurons which can receive signals, process them and transmit signals to connected neurons. The connections are referred to as weights and mimic synapses; they govern the transmission strength of signals to other neurons and can be adjusted. These networks typically consist of multiple layers and as such this approach is referred to as deep learning. In these implementations of neural networks, the synaptic weights are stored in the separated memory unit and need to be repeatedly loaded into the processing unit to compute the desired output to the next layer of neurons. Consequently, the performance of software-based ANNs is fundamentally limited by their hardware, they consume considerable energy and space and they cannot efficiently simulate the brain’s level of parallel processing[9, 10].

So far, several large-scale neuromorphic hardware architectures based on complementary metal-oxide semiconductor (CMOS) technology have been developed
that are either digital, such as IBM TrueNorth\textsuperscript{2}, Intel Loihi\textsuperscript{11} and SpiNNaker\textsuperscript{12} or employ a combination of digital and analogue signals, such as BrainScaleS\textsuperscript{13} and Stanford Neurogrid\textsuperscript{14}. These architectures have shown the potential to outperform CPUs in terms of efficiency by several orders of magnitude. Some of these neuromorphic chips can operate with powers on the milliwatt scale, in contrast to the tens or hundreds of watts consumed by traditional chips. These CMOS implementations of neuromorphic architectures require a large number of components and complex circuitry to emulate neurons and synapses and hence, if they would be scaled up to the human brain, the power consumption is still expected to be at least three orders of magnitude higher than the approximately 20 W used by the brain\textsuperscript{15}.

To bridge this gap, we can build devices that more closely resemble the functionalities of the neurons and synapses that make up the brain than the CMOS-based transistors currently used. Specifically, we can use the intrinsic physical properties of novel electronic devices to naturally emulate the neural and synaptic functionalities in hardware.

1.2 Memristors

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{memristors.png}
\caption{Memristors: (a) Relations between the four electrical circuit variables (voltage, $V$, current, $I$, charge, $q$ and magnetic flux, $\phi$) and the ideal circuit elements (resistor, capacitor, inductor and memristor) associated with pairs. Based on \textsuperscript{16}. (b) Different switching mechanisms that can give rise to memristive behaviour.}
\end{figure}
Various new electronic elements have been explored in this regard. Among them, memristors, which were first proposed as fundamental circuit elements based on symmetry arguments, illustrated in Fig. 1.2(a)[16, 17]. There are four fundamental circuit quantities: voltage ($V$), current ($I$), charge ($q$) and magnetic flux ($\phi$) and six possible equations to establish a relation between two of these variables. Two equations define current and voltage in terms of charge and flux and three others describe the properties of the well-established circuit components (resistor, capacitor and inductor). The memristor was introduced as a fourth component to fulfil the missing link between magnetic flux and charge. $q$ is the time integral of $I$ and similarly using Faraday’s law, $\phi$ can be expressed as the time integral of $V$; using these definitions, the memristors can be seen to provide a time-dependent link between voltage and current. Instead of having a constant resistance, they regulate the flow of current based on the amount of charge that has previously flowed through them allowing them to retain memory without power. In other words, their resistance can be programmed and remains stored in the absence of power.

Depending on the time scale of memory retention, the behaviour can be classified as either volatile (memory disappears at zero bias) or non-volatile (memory is retained at zero bias). Non-volatile (or partially non-volatile) memristors are suitable for memory applications and can be used as electrical synapses wherein they can be used as continuously tunable weights if they show analogue behaviour. They can provide an output current that is a conductance-weighted function of the input voltage. Volatile memristors, on the other hand, have interesting temporal behaviour and can be used to perform non-linear transformations of the input, such as thresholding or spiking, making them promising candidates for realising electrical neurons[5].

The realisation of such devices requires a physical change to occur within a material that can be triggered by an externally applied stimulus, often voltage or current, that can be measured as a change in resistance. A wide range of mechanisms have been investigated that give such an effect, some of which are highlighted in Fig. 1.2(b)

1.2.1 Phase Change

Phase change materials can switch between an amorphous state with high resistance and a crystalline state with lower resistance, by virtue of Joule heating. The resistance can be controlled by shaped voltage pulses. When a low voltage pulse is applied for an extended time, the material gets heated to its crystallisation temperature where it melts if it is allowed to cool down slowly it crystallises into a low resistance state. To increase the device resistance, higher and shorter pulses are used that rapidly melt part of the material at high temperatures if the material is quenched and
rapidly cools down it becomes amorphous\cite{18, 19}. The most widely studied class of materials for this purpose are compounds of Ge, Sb and Te\cite{20, 22}.

### 1.2.2 Ferroelectric

A ferroelectric tunnel junction (FTJ)\cite{23–25} consists of a thin ferroelectric layer between two metal electrodes. Electrons tunnelling through the FTJ are repelled or attracted, depending on the polarity of the ferroelectric layer and hence the transmitted tunnelling current is modulated by the ferroelectric polarisation direction of the insulator. Hence, a sufficiently large voltage can be used for writing and subsequently, a smaller voltage can be used to read in a non-destructive way. One of the most widely used materials for FTJs is hafnium oxide (HfO$_2$)\cite{26} and it has been used in various neuromorphic applications\cite{27, 28}.

### 1.2.3 Spintronic

Spin-based electronic devices typically include two ferromagnetic layers separated by a nonmagnetic spacer layer, which can either be a metal (spin-valve)\cite{29} or an insulator (magnetic tunnel junction (MTJ))\cite{30}. The relative magnetisation alignment determines the resistance through the stack. The magnetisation directions can be manipulated by an external magnetic field or current. The latter can either be realised using spin transfer torque (STT). When electrons flow through the pinned layer, they are scattered and the current becomes spin polarised in the direction of the magnetisation. The transmitted spin-polarised electrons exert an angular momentum (torque) on the other ferromagnetic layer which can be used to manipulate its magnetisation direction. The magnetisation can also be controlled through spin-orbit torque (SOT). An in-plane current flowing through a heavy metal layer will cause a spin accumulation at the interface which exerts a spin angular momentum on a neighbouring ferromagnetic layer.

These mechanisms allow MTJs to act as spintronic synapses, in which the resistance through the device can be altered using current pulses and the weight is retained due to the non-volatile nature of magnetisation. Depending on the domain structure of the ferromagnetic layers used, these memristors can either be bistable\cite{31, 32} or analogue\cite{31–35}.

Spintronic devices can also be used to emulate neurons. Using torques, MTJs can be used to transform direct current (dc) inputs into an oscillating voltage output with a frequency that depends non-linearly on the injected current. If the energy barrier between the different states is sufficiently low, thermal noise may be able to include sufficient to induce random fluctuations, allowing the mimicking of stochastic neurons\cite{36, 37}.
1.2.4 Nanoionic

In general, this mechanism is found in metal/dielectric/metal structures and the resistive switching relies on the migration of ions originating either from the dielectrics or electrodes. Depending on the spatial location of conducting path, this mechanism can be categorised as filamentary, where the switching results from the formation and rupture of a conductive filament or interfacial, in which the resistive switching occurs at the interface between an electrode and the oxide[38].

The mechanism of filamentary switching depends on the type of ions that make up the conduction path and is either referred to as electrochemical metallisation (ECM) or valence change (VC). ECM makes use of the electrochemical metallisation of active metal species typically originating from (one of) the electrodes. Metal cations, generated from one of the electrodes, are electrically dissoluted and migrate towards the other electrode where they recrystallise under the influence of an external electrical bias. VC, on the other hand, makes use of anion vacancies, such as oxygen vacancies that tend to originate from the dielectric layer. In dielectrics with at least one transition-metal species, anion vacancies can react when a voltage is applied so that the valence state of the transition-metal cations is changed. These defects can then diffuse under the electrical field and form a connection between the two electrodes. As-prepared (or virgin state) devices tend to be in a highly resistive state the application of a high voltage stress during an irreversible electroforming process leads to partial dielectric breakdown resulting in a low-resistance state (LRS). The subsequent reversible switching can be either ambipolar (or unipolar) or bipolar. In unipolar switching, the switching direction depends on the amplitude of the applied voltage but not on its polarity. A device can switch to a high resistance state (HRS) by applying a threshold voltage (‘reset process’) and switch back to an LRS by applying a larger voltage while limiting the current by utilising current compliance or by adding a series resistor. In bipolar resistive switching, on the other hand, the polarity of the applied voltage controls whether the device switches from LRS to HRS or vice versa[38].

In contrast, the interfacial (or area-dependent) type path, relies on material changes that occur under the influence of an applied electric field in a region localised close to the interface. This mechanism is usually bipolar and found between metals and semiconducting perovskite oxides. Key mechanisms driving this effect have been identified as electrochemical migration of oxygen vacancies[39–44], trapping of charge carriers (electrons or holes)[45,49] and Mott transitions induced by carriers doped at the interface[38,50–53].
1.2.5 Mott Insulators

Insulator–metal or metal-insulator transitions are phase transitions characterised by drastic changes in electrical properties, which may be paired with structural and magnetic transitions[54]. These phase transitions can be triggered by thermal energy, Joule heating or optical stimuli, and the system’s state can be probed electrically, optically or magnetically. This is typically a volatile effect where a localised temperature increase converts the heated region from a metallic (insulating) state to an insulating (metallic), giving rise to the abrupt resistance change. Reducing the applied current or voltage decreases the local temperature to below the transition temperature, recovering the starting state. Often, this is paired with the observation of negative differential resistance (NDR), a phenomenon where the current decreases with the increasing applied voltage. This highly nonlinear effect has attracted attention for applications such as neural-inspired signal processing and nonlinear oscillating circuits[55, 56]. Materials in which these effects have been observed include VO\(_x\)[54, 57–59], NbO\(_x\)[60–62], La\(_{0.33}\)Sr\(_{0.67}\)MnO\(_3\)[63, 64] and TbMnO\(_3\)[65].

1.3 Applications

1.3.1 Binary Memory

Memristive devices with two stable resistive states can be utilised for non-volatile memory where the low resistance state (LRS) represents the binary one and the high resistance state a binary zero (Fig. 1.3(a)). While such non-volatile memories have been commercialised since 2021, they have to fulfil stringent requirements to be compatible with the current integrated circuits. These requirements include low writing voltages (<3 V), fast switching time (<10 ns), high endurance (>10\(^{10}\) cycles), resistance ratio >10, and long retention times (>10 years). Currently, phase change memristors are the most widely used for this purpose, but manufacturing costs are significantly higher than that of the commonplace memories because their integration requires custom back-end-of-line fabrication outside the standard processing employed in CMOS[66, 67].

1.3.2 Advanced Computation

A characteristic of memristors that can be exploited for computation is accumulative behaviour; a sequence of pulses applied to a device can give rise to a progressive increase or decrease in the conductance, allowing devices to be used as synaptic weights in machine learning models.
1.3. Applications

Figure 1.3: Applications of memristors. (a) Binary memory: A stable high and low state can be used to represent a binary 0 and 1, respectively. (b) Matrix-vector multiplication (MVM): an array of memristive devices can be used to perform computation in memory without moving the data where the elements of the matrix are correlated to conductances (G), and the input and output vectors correspond to voltage and current vectors, respectively. (c) Security: intrinsic stochastic behaviour of devices gives rise to unpredictable cycle-to-cycle variations. (d) Mobile communications: the low and high resistance states can be used to either transmit or attenuate radiofrequency (RF) signals.

An array of memristive devices can be used to perform computational tasks in memory without moving the data. Notably, matrix-vector multiplication (MVM), i.e. $\mathbf{A}\mathbf{x} = \mathbf{b}$ (Fig. 1.3(b)). The elements of the matrix $\mathbf{A}$ can be linearly correlated to conductances (G) and mapped onto a crossbar configuration. The values of the input vector $\mathbf{x}$ can be mapped to voltages supplied (v) to the rows of the crossbar. By virtue of Ohm’s law for multiplication at each crossing point and Kirchhoff’s law for accumulation at each node, the resulting currents (i) along the columns is proportional to the result of the computation, $\mathbf{b}$.

1.3.3 Security

Modern security applications, such as multi-factor authentication, rely heavily on random number generators. Currently, these strings of numbers are typically generated through software algorithms, but this makes them prone to being hacked. Instead, the intrinsic variability of memristive devices between cycles (Fig. 1.3(c)) as well as resistance fluctuations over time could be used to generate truly unpredictable strings of bits. Given that these fluctuations depend on atomic-level variations, they are impossible to predict\textsuperscript{[67–71]}. 
1.3.4 Mobile Communication

Memristive devices with two stable states could be used as passive radiofrequency (RF) switches\cite{72,75}. When such a device is in its LRS, it can transfer an RF signal. In its HRS, on the other hand, it produces a capacitance effect that blocks the signal (Fig. 1.3(d)). Currently, silicon-based transistors are primarily used for this, but their volatile nature means they consume energy even when they are idle; while memristors would only require energy during the switching operation\cite{67}.

1.3.5 Probabilistic Computing

![Figure 1.4: Bits for computing: binary bits, used in traditional computing, have a deterministic value that can be used to represent information in a binary code and can be realised using stable magnetic tunnel junctions (MTJs). Quantum bits (q-bits) are in a superposition of 0 and 1 and can be represented by single spins. Probabilistic bits (p-bits) are an intermediate type and are fully classical, but fluctuate between 0 and 1 and can be realised through unstable MTJs.](image)

Modern computing is based on deterministic binary bits and can be either ‘0’ or ‘1’. Quantum computing, on the other hand, makes use of quantum bits (q-bits) which are in a superposition of ‘0’ and ‘1’. Probabilistic bits (p-bits) can be viewed as an intermediate type; they are classical, but their state fluctuates in time between ‘0’ and ‘1’. These three types of bits are compared in Fig. 1.4. Quantum computing is expected to perform certain tasks considerably more efficiently than classical computing but requires cryogenic temperatures. Hence, probabilistic computing offers an alternative solution to tasks such as Bayesian inference\cite{76}, invertible logic\cite{77} and integer factorisation\cite{78} at higher temperatures\cite{79}.

One way to represent bits is using magnetic tunnel junctions where the (anti)parallel alignment can be used as the (‘0’) ‘1’ state. If the energy barrier separating the two states is sufficiently large, these bits will be stable. If the energy barrier is lowered,
however, due to (thermal) noise the device can switch back and forth between the two states where the rate and time spent in each state depends on the energy landscape\textsuperscript{79}.

1.4 Challenges

1.4.1 Materials

Figure 1.5: Radar charts comparing performance of four types of memristors. Filamentary (red), phase change (green), spintronic (dark blue) and ferroelectric (light blue). Based on data from\textsuperscript{80–86}.

Given the large number of possible applications, the properties required of a memristive device may differ. Due to their reliance on different physical switching mechanisms, different types of memristors offer distinct properties. The four most common types of compared in Fig. 1.5.
With the goal of building large-scale networks capable of processing large volumes of data in mind, scalability is an important consideration. This aspect considers device size, cell area (the area one device and any peripheral circuit elements consume), and packing density (how close devices can be placed). In this area, filamentary switching and PCM devices have demonstrated the best characteristics due to their simple devices design and ease of fabrication. Challenges related to the epitaxial growth of ferroelectric materials and spin-dependent scattering limit the scalability of FTJs and MTJs. Additionally, spintronic devices utilising SOT tend to be three-terminal devices; while this provides additional benefits and functionalities, it increases the cell size.

The speed and energy of the write/read operations are important performance parameters for overcoming the von Neumann bottleneck. The writing operations of PCMs require large currents to melt the material and a relatively long time is required for crystallisation, especially for switching from the HRS to the LRS. Switching the polarisation of a ferroelectric material entails high voltages. Consequently, filamentary devices and MTJs demonstrate superior performance in terms of low writing power over PCM and FTJs.

For reliable operation and ensuring devices can be switched repeatedly without failure, high endurance is favourable. In this respect, all four types outperform flash ($10^5$ cycles) but have a lower endurance than DRAM ($10^{15}$). In this area, spintronic devices show the best performance while FTJs perform the worst due to ferroelectric ageing and fatigue[87, 88].

Data retention in PCMs can be difficult to attain as it depends strongly on the material composition of the PCM and it is often observed that over time the HRS drifts as the amorphous phase recrystallises. However, through composition optimisation, long retention times have been demonstrated in PCMs, sometimes at the cost of other performance parameters[89]. Ferroelectric materials are typically the worst candidates for retention due to polarisation relaxation effects.

The on/off ratio may be important for some applications; high ratios can be favourable for better clarity of states and in analogue devices provide a larger dynamic range. However, for applications such as two-state memory, a ratio of 10 is enough for reliable operation[67] and for some purposes, large differences in the currents in different states may not be suitable as it could be difficult to match the output current to peripheral circuit elements over the full range. Spintronic devices tend to exhibit relatively low ratios. This is because the on/off ratio of MTJs is highly dependent on the spin polarisation, which is sensitive to factors such as temperature, material defects and interface imperfections, due to their effect on spin-scattering. MTJs also show the worst performance in terms of multilevel operation while the highest number of distinguishable resistance states have been demonstrated in filamentary memristors.
1.4. Challenges

The desired level of stochasticity depends greatly on the application. Low stochasticity is typically favoured for cognitive tasks in ANNs where the recognition accuracy is improved. Additionally, while neuromorphic computation is relatively robust to hardware defects, and in some cases a small amount of noise in neuromorphic computing aids with learning and information processing, significant memristor variability can be an issue\[82\][90]. If each device on a large chip behaves differently, programming individual devices to a specific state becomes almost impossible. For tasks such as data encryption and random number generation, on the other hand, a certain degree of variability is inherently crucial to the task. PCMs have the highest stochasticity due to variations in the atomic configurations of the amorphous phase after each reset operation\[91\][92]. The lowest stochasticity has been demonstrated by spintronic memristors. Their performance depends on their energy landscape; when the energy barrier separating the parallel and antiparallel state of an MTJ is high it will exhibit low stochasticity, but if the energy barrier is lowered, the behaviour can be made more stochastic\[76\][78][79].

There are several important aspects of performance related to symmetry and linearity. Symmetry/linearity in (i) the current-voltage response and (ii) the change in resistance induced by pulses. Asymmetry and non-linearity in the current-voltage response can be useful for avoiding sneak path currents in crossbar architectures. However, when concerned with the change in resistance with supplied pulses it is often stated that the ideal memristor response should be linear and symmetric, meaning that each pulse changes the weight by the same amount, independent of the current state. Filamentary memristors tend to exhibit low linearity due to the nonlinear nature of the formation and rupture of the conductive filaments. In contrast, FTJs, exhibit better linearity due to the more uniform nature of the switching mechanism. The applied electric field is present in all regions of the material and the polarisation is switched in all areas, resulting in a more linear relationship between the input voltage and the output resistance. The highest linearity has been found in MTJs. Due to the symmetric nature of magnetisation/polarisation reversal processes MTJs and FTJs show more symmetric behaviour than PCMs, where the reset process is abrupt, and filamentary devices, which are subject to a more abrupt set operation.[80][86].

It should be noted that optimising material performance is often a trade-off. For example, increased linear weight update is likely to come at the cost of lowering the dynamic range\[93\], increasing the device retention may also increase the variability\[94\], or there may be a trade-off between the on/off ratio and the stability/reliability\[95\]. Hence, even within a class of memristors, not all state-of-the-art properties are likely to be present in the same device. Depending on the task, some properties are more important than others and hence the choice of material should match the application.
1.4.2 Network Integration

The latency is the time it takes to access a device and becomes an important consideration when integrating devices into a network. Resistance of peripheral circuitry can result in a significant voltage drop across the wires, increasing the latency\[90\]. Similarly, sneak path currents (currents that flow through non-selected devices during reading and writing operations) should also be considered. Both these factors can affect the voltage supplied to the memristor which can affect the read/write operations. To avoid the latter, highly non-linear selector devices can be integrated with each memristive device to isolate a specific memristive element. While higher nonlinearity reduces the latency, selectors have their own variability and their integration increases the complexity, size and cost of the system\[90, 96\]. An alternative solution is using self-rectifying characteristics of memristors to suppress sneak path currents, and hence bypass the need for a designated selector device. This is possible if the memristor itself has sufficient self-rectification or non-linear characteristics.

1.4.3 Interfacial Switching

While filamentary switching is perhaps the most widely studied switching mechanism, control of multi-level switching, variability and intrinsic stochasticity are standing issues. Interfacial devices have the potential to show less variability and precise analogue tuning of the conductance. These devices are less widely investigated and hence these properties are not characterised on a high statistical basis. The retention is typically lower than for filamentary devices. The current scales with the area and as a result the power is expected to reduce with downscaling. Typical devices, however, have a large area and scaling them to the nanoscale is an open issue. The fabrication and characterisation of interfacial memristors need further investigation. Furthermore, while substantial effort has gone into developing models for filamentary switching, simulation models for interfacial switching are not widely available and should be developed\[97\].

1.4.4 Spintronic Memristors

To achieve the high packing density that will be required of spintronic devices in a network, it is important that the individual devices have perpendicular magnetic anisotropy (PMA). The most widely used materials for PMA are composed of heavy metals where, to overcome shape anisotropy, either the ferromagnetic layers have to be ultra-thin or additional layers are required\[32, 98, 99\]. This leads to overall complex MTJ stacks with a large number of layers. To be able to address each device independently, we also need a switching mechanism that utilises current, rather than
a magnetic field. In this respect, SOT is the most promising candidate and enables switching the magnetisation of a ferromagnetic layer using an in-plane current. A layer with perfect PMA, however, is rotationally symmetric to an in-plane current, prohibiting deterministic switching. To break the in-plane symmetry, either an external magnetic field can be applied along the current direction, additional layers can be added to provide an internal magnetic field via exchange bias or stray field, or by creating a wedge structure. These complex device designs may complicate the integration of spintronic memristors in large-scale networks.

1.5 Complex Oxides

![Complex oxides](image)

**Figure 1.6: Complex oxides.** (a) The strong coupling between the orbital, charge, lattice and spin degrees of freedom make these materials highly tunable. (b) Close lattice match allows epitaxial growth where the substrate exerts a strain on the film which can alter its properties. (c) Oxygen vacancies and dopant atoms can be used to tune the characteristics.

Complex oxide perovskites, ternary oxides with an ABO$_3$ structure, have attracted great research interest over the past decades. They have been shown to exhibit a broad spectrum of interesting phenomena, including superconductivity, (anti)ferromagnetism, (anti)ferroelectricity, multiferroic properties and colossal magnetoresistance. The ideal cubic perovskite structure is comprised of a
larger cationic species on the A site with 12-fold cuboctahedral coordination and smaller cations on the B site with 6-fold coordination surrounded by an octahedron of $O^{2-}$. The symmetry depends on the Goldschmidt tolerance factor $t$:

$$t = \frac{r_A + r_0}{\sqrt{2(r_B + r_0)}},$$

(1.1)

where $r_A$, $r_B$ and $r_O$ are the ionic radii of A, B and O, respectively. Central to the work in this thesis are SrTiO$_3$ (STO), for which $t = 1$, giving it an ideal cubic structure and SrRuO$_3$ (SRO) with $t \approx 0.991$, resulting in an orthorhombic unit cell.

The physical properties of these oxides are mainly derived from strongly correlated d electrons because the s electrons of constituting transition metal are transferred to the oxygen ions. The constrained nature of these d electrons gives rise to a strong coupling between the charge, spin, lattice and orbital degrees of freedom (Fig. 1.6(a)) which is the underlying origin for many of the interesting phenomena found and additionally makes these materials highly tunable [113].

Their properties can, for example, be altered by small changes in their stoichiometry, through strain (Fig. 1.6(b)), by gating or by adding dopant atoms (Fig. 1.6(c)). Specifically, in this thesis, we used Nb as a dopant. STO is a wide bandgap (3.25 eV [114]) insulator; when some of the Ti ions are replaced by Nb, it becomes an n-type semiconductor. Using the hydrogenic theory of shallow donors, the donor binding energy, $E_D$ is given by:

$$E_D = -13.6 \text{ eV} \left(\frac{m_e^*}{m_e}\right) \left(\frac{1}{\epsilon_r}\right),$$

(1.2)

where $m_e^*$ and $m_e$ are the effective and free-electron masses, respectively and $\epsilon_r$ is the dielectric permittivity. STO has a high and temperature-dependent effective mass of between (1-10)$m_e$ [115], resulting in an $E_D$ around 1.5 meV at 300 K ($k_BT \approx 26$ meV) and 0.2 $\mu$eV ($k_BT \approx 360$ $\mu$eV) at 4.2 K. Consequently, shallow donors are ionised at all temperatures of interest, resulting in the absence of carrier freeze-out in doped STO and an almost temperature-independent carrier concentration [116, 117].

In addition, these transition metal oxides can play host to oxygen vacancies (Fig. 1.6(c)), which can further alter their properties. In STO, for example, these vacancies, which tend to be electron donors, can have carrier mobilities that are significantly higher than those of impurity dopants [118]. Their presence in many oxides paired with the fact that they behave as mobile donors that can be controlled electrically has made them an important factor underpinning resistive switching in many materials.

1.6 Motivation and Outline/This Thesis

The research presented in this thesis explores complex oxides as a platform for novel computing architectures. Chapters 3, 4 and 5 study interfacial memristors based on
metal contacts on Nb-doped STO (Nb:STO). Chapters 6 and 7 explore a spintronic approach to neuromorphic computing using the anisotropy control of ferromagnetic SrRuO$_3$ layers.

This thesis consists of the following chapters:

- **Chapter 2** presents some basic physical concepts relevant to the work presented in the thesis. Starting from a general introduction to metal/semiconductor interfaces, including barrier formation and transport across the interface. The next part focuses on spintronic concepts starting from the spin-orbit coupling and the spin-Hall effect, which are relevant for understanding spin-orbit torque. The second half of the chapter introduces several relevant device fabrication techniques and explains some important measurement techniques and setups.

- **Chapter 3** introduces Nb:STO interface memristors. In this chapter, we study the properties of large-area junctions. We also model the device behaviour in order to develop relevant learning algorithms.

- **Chapter 4** explores the area dependence of Nb:STO memristors. We find that the memory window increases with area reduction which we attribute to a controlled enhancement of the electric field around the device perimeter. This is supported by finite element simulations. In addition, we use scanning transmission electron microscopy (STEM) to directly image the interface, showing a homogeneous layer of oxygen vacancies can be controlled by an applied field.

- **Chapter 5** studies the effect of varying the doping concentration of the substrate. We further model the Schottky barrier profile to link the observed trends with electronic transport across the interface.

- **Chapter 6** investigates current-induced magnetisation modulation in tailored ferromagnetic layers interfaced with Pt heavy metal layers. By growing ferromagnetic SRO layers on STO layers with different orientations, we show that the magnetic anisotropy can be manipulated to be perfectly out-of-plane or tilted. First and second harmonic magnetoresistance measurements highlight the differences in anisotropy and the presence of spin-orbit torques. We propose a three-terminal spintronic memristor, with a magnetic tunnel junction design, that utilises SOT as a writing mechanism and depending on the anisotropy shows either probabilistic or deterministic behaviour.

- **Chapter 7** integrates SRO layers with substrate-controlled anisotropy into stacks to construct all-oxide magnetic tunnel junctions. Characterisation of the structural and magnetic properties of multilayer stacks demonstrates that the magnetically decoupled electrodes can be grown epitaxially with a strong out-of-
plane component. Large tunnelling magnetoresistance and spin polarisation are attained that persist up to high bias and temperature.

- **Chapter 8** summarises the most important findings of this thesis and discusses them in light of beyond von Neumann computing. Foreseeable challenges and potential applications are discussed. We propose a crossbar architecture suitable for network integration of the interface memristors discussed in Chapters 3-5.
References


1. Introduction


1. Introduction


1. Introduction


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1. Introduction


1. Introduction


