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Networks of Functional Metal Oxides Towards Neuromorphic Materials

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INTRODUCTION

1.1. MOTIVATION & BACKGROUND

Artificial Intelligence (AI) has seen a massive increase in importance in the past few years. AI and deep learning networks are used for a multitude of applications, such as image and speech recognition, social networks, finances, medicine, cybersecurity, gaming and language models, such as ChatGPT (as an example that came available to the public recently). [1–3] Most of these AI systems run on supercomputer clusters which are based on traditional central processing units (CPU), accelerated by graphics processing units (GPU), and result in high power consumption for both the operation and training phase of these deep neural networks.

Conventional computers rely on digital information processing using transistors, which are on/off switches that are fabricated on Si wafers, following the *so-called* Complementary Metal–Oxide–Semiconductor (CMOS) technology. The design of these computers is based on the von Neumann architecture, where data processing and data storage are physically separated. This leads to the 'von Neumann bottleneck': the continuous transport of data between the processor and the memory is costly in both time and energy consumption and limits the speed at which data can be transported. In order to overcome this bottleneck, researchers are taking inspiration from the brain and are looking for solutions in which data storage and processing are co-localized. Even though the functioning of the brain is not yet fully understood, it seems clear that there are no separate regions for memory and information processing. [1] The brain employs parallelism on a massive scale, and its operation is based on the creation and transmission of electrical signals (spikes), such that the information is encoded in the time between spikes, in an analog manner. Neurons and synapses are responsible for data processing and data storage in the brain. About 10^{11} neurons are highly interconnected in a complex and adaptable network, forming of the order of 10^{15} synapses. The brain consumes about 20 W of power to operate (and is constantly learning), whereas a deep learning supercomputer cluster of a similar size (in terms of number of connections) consumes about 7.9 MW of power (almost a factor 400.000 more). [4]

The idea of brain-inspired - or neuromorphic - hardware has been around since the 1980s (put forward by Carver Mead), [5,6] but the relatively small amount of data that computers needed to deal with at that time limited the general interest in this technology. This has now drastically changed and neuromorphic technology is developing fast. The current high-end neuromorphic chips, such as the ones developed by IBM (TrueNorth) and Intel (Loihi) are based on the crossbar array structure, where the neurons and synapses are formed out of many transistors. [4,7–10] While these chips already outperform conventional computing in terms of power consumption for certain tasks, the amount of transistors used in these chips requires large chip areas limiting the functionality of these chips. For example, the Loihi 2 chip features 1 million neurons and 120 million synapses, but it requires 2.3 billion transistors in order to achieve this. [10] To progress the field and reduce energy consumption even further, it is necessary to explore beyond traditional CMOS structures to find materials and novel device structures that are specifically tailored to achieve neuromorphic computing in hardware. This research into new materials for brain-inspired hardware has really taken off since HP labs reported in 2008 that resistive switching devices were the realization of the memristor (memory resistor), a circuit element theoretically proposed by Leon Chua decades earlier. [11,12]

Memristors are devices with multiple available resistance states, that use intrinsic prop-

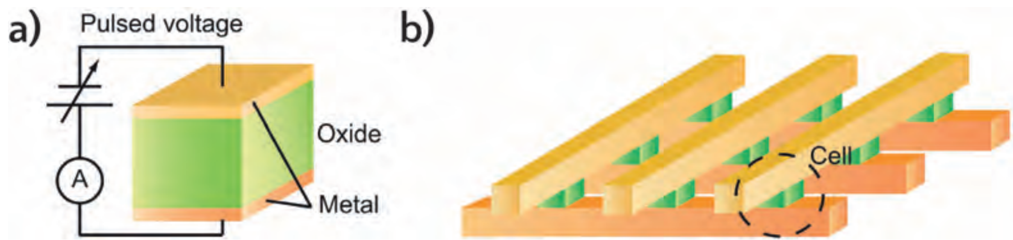

Figure 1.1 | a) Schematic representation of a memristor cell within the crossbar array structure, with a metal oxide as the active material. b) Schematic representation of a crossbar array structure in which many cells are arranged in a matrix format. Adapted from Sawa, Materials Today, **11**, 28 (2008).[22] Copyright 2008, with permission from Elsevier.

erties, based on their underlying physics or chemistry phenomena, to emulate functions of biological synapses in order to enable energy-efficient, in-memory computing. Resistive switching in thin layers has been investigated for their use in non-volatile resistance random access memory (ReRAM), as an alternative for Flash memory. These devices are based on a metal-insulator-metal (MIM) structure in which the resistance of the insulating layer (metal oxides, chalcogenides, or organic compounds) can be electrically switched, typically involving redox reactions and nano-ionic transport.[13–23] or phase changes.[24–28] It became apparent that the hysteretic current-voltage characteristics and non-volatile resistive switching observed in these two-terminal ReRAM devices could actually be understood as memristive behaviour.[12] This led to the realization that these devices could be used beyond digital information processing (ReRAM) and could be applied in learning networks that require synapse-like functions - brain-inspired hardware.[12] Typically, these networks consist of two terminal MIM crosspoint switches, organized in a crossbar array, where the I-layer is typically a metal oxide or a phase change material (PCM). A crossbar array is essentially a mesh of devices, in which electrode lines are ordered perpendicularly to form a matrix (Figure 1.1). To switch the devices between different resistance states, a voltage is applied to the end of two orthogonal wires in order to access the cell intersecting both lines.[22,23,29] Thanks to Kirchhoff's laws the voltage inputs and current outputs on the perpendicular lines produce the multiplication of voltage vectors and conductance matrices. Therefore, memristive crossbar arrays are ideally suited for matrix-vector multiplications and form a hardware analogue to the software artificial neural networks (ANNs), such that the elements of one conductance matrix are equivalent to the weights of one layer in an ANN, saving large amounts of computing power.[30–34] Generally, crossbar arrays are fabricated with node sizes in the order of a few tens of nanometers,[35] with the smallest reported nodes to date being: the 10x10 nm HfO_2 nodes from IMEC, fabricated through a 65 nm CMOS process;[36] the 8x8 nm TiO_2 nodes from Pi et al., fabricated through nanoimprint lithography,[37] and their 2x2 nm $TiOx/HfO_2$ nanofin-based nodes.[38]

As mentioned above, there has already been a lot of attention paid to designing neuromorphic hardware with new device architectures and, in parallel, to finding new materials that exhibit memristive properties. Among the different types of reported materials, the most mature ones are the chalcogenide phase change materials and the metal oxides.[39] These materials classes are already used for applications in the chip industry and are, therefore, very

interesting to investigate for in-memory computing applications. The metal oxides being a very diverse and versatile class of materials, they offer a lot of possibilities and great promise for applications in emerging memories.[39] Part of the interest in metal oxides stems from the integration that of some of the simple metal oxides (i.e., SiO_2 and HfO_2) already have into the semiconductor industry.[40] Moreover, a plethora of different physical responses are accessible within the (complex) metal oxides class, since the materials properties can be (easily) tuned by changing parameters such as oxygen content, doping, and strain.[41–43] An additional advantage of these materials is that the growth of thin film metal oxides has been widely studied and optimized over the past decades. Techniques such as Molecular Beam Epitaxy (MBE), Sputtering, Pulsed Laser Deposition (PLD), and Atomic Layer Deposition (ALD), allow for the growth of atomically controlled materials.[42,44–48]

Since many (complex) oxides require strain engineering to achieve some of the desired properties, they are not easily compatible with the silicon-based semiconductor industry, as special single crystalline substrates are often required to obtain films with the right properties.[42] One way to achieve chip integration in these cases is through stack inversion and wafer bonding: here the metal oxide is grown on a substrate, then the stack is inverted such that the top layer of the stack is bonded to a silicon wafer. Finally, the original substrate is removed through etching.[49,50] However, in view of ease- and cost of fabrication, materials that can be directly grown on silicon will likely be preferred by industry. Additionally, (epitaxial) oxide growth often requires high temperatures during the growth and annealing steps. While this is not an issue for lab-scale research purposes, it can become problematic when these materials need to be integrated in device fabrication processes, especially for Back-End-Of-Line (BEOL) processes where the maximum processing temperature is in the range of 400 °C.[39,51–53] Exceeding this temperature limit risks damaging the entire device stack. However, some recent developments may lift these limitations in the future: low temperature ALD has been reported for the epitaxial growth of rare earth nickelates on $SrTiO_3$.[52] With further development of this technique, this might also apply to other metal oxides, allowing for better control of the properties of metal oxides and their integration into the semiconductor industry.

1.2. BACKGROUND ON MEMRISTIVE DEVICE OPERATION

In this thesis we create network structures made of different metal oxide materials that have already shown some form of resistive switching in literature: $BiFeO_3$, $SrTiO_3$, HfO_2, $La_{0.7}Ca_{0.3}MnO_3$ (Chapter 4), and $La_{0.7}Sr_{0.3}MnO_3$ (Chapter 5). While the intent is to ultimately use these novel materials for neuromorphic hardware, the focus of this work is on the fabrication of these structures and their characterization. Only in Chapter 5 we hint at possible memristive behaviour in one type of networks. Even though the memristive device operation is not the focus of this thesis, it is the main motivation for future work and, thus, we introduce redox-based (or ion-based) resistive switching (Section 1.2.1), as this is the main type of resistive switching applicable to the materials discussed in this thesis.

Other switching mechanisms, such as phase change-based switching (one of the most integrated classes of resistive switching), spin-based switching, and ferroelectric memristive switching are not discussed here, but we would like to refer the reader to the following

references for more information.[24–28,54–61]

1.2.1. REDOX-BASED RESISTIVE SWITCHING

Redox-based resistive switching devices rely on redox reactions for their operation. Generally, these devices consist of an active layer (oxide, ionic solid, or chalcogenide) that is sandwiched between two electrodes. The redox processes will occur at the electrodes, in the active layer, or as a combination of these two.[54] The most common switching type for redox-based devices is filamentary switching, by which a conductive filament is formed in the active layer between the two electrodes. The current-voltage (I-V) characteristics of these devices depend on the state of the conductive filament: the device presents a high resistance state when the filament is not fully formed and a low resistance state when the filament is fully formed. Due to the nonvolatile state of the filament formation, these devices are attractive for applications in nonvolatile memories.

Within the subclass of filamentary switching, there are three different types of redox-based switching: electrochemical metallization (ECM), valence change metallization (VCM), and thermo-chemical metallization (TCM) (Figure 1.2a). In ECM devices, a conductive filament is formed under the application of an electrical bias, due to the migration of metal ions from a electrochemically active electrode (such as Ag or Cu) to the counter electrode. The filament is formed across the metal oxide or ionic solid, which act as a solid electrolyte for the ions migrating between the electrodes.[20] In VCM devices,switching relies on the movement of oxygen anions, and their accompanying oxygen vacancies, within the metal oxide layer, and the subsequent formation of a conductive filament: electrons hop between the oxygen vacancies, creating a conduction channel if the oxygen vacancies percolate across the thickness of the active layer. Finally TCM devices rely on thermochemical breakdown of the active layer through Joule heating, resulting in the formation of a conductive filament created from the active layer. In a TCM device the electrodes are inert and the filament is formed by the oxidation and reduction of active layer, forming a metallic filament.[54] An electroforming step can be required for filamentary switching devices before resistive switching can be observed. During electroforming, the growth of the conductive filament is initialized by applying a relatively high voltage to the device. Subsequent switching can then be done using lower voltages, since the filament only needs to partially dissolve during cycling to give rise to different resistance states.

A non-filamentary switching type that can be observed for redox based resistive switching is known as interface-type switching. In this case the switching occurs homogeneously at the interface between the active layer (metal oxide) and the electrode (Figure 1.2b). Migration of oxygen ions changes the width of the tunnel barrier, affecting the resistance state of the device, and giving rise to an area dependent process, unlike in the filamentary conduction cases.[22,54,62,63] It should be noted that p- and n-type devices behave differently under reductions-oxidation: the conductance increases with an increasing concentration of oxygen vacancies near the interface for n-type materials, while it decreases for p-type materials.[63] The advantage of interface-type switching is that electroforming is not required for device operation and there is a gradual set/reset slope, allowing access to a larger number of intermediate resistance states and in the case of filamentary memristors.[64]

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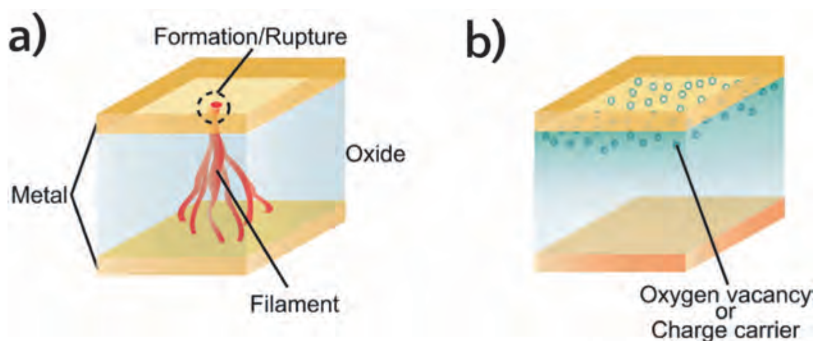

Figure 1.2 | Schematic cell structure and operation principle for a) filamentary-type and b) interface-type resistive switching. Reprinted from Sawa, Materials Today, **11**, 28 (2008).[22] Copyright 2008, with permission from Elsevier.

1.3. MATERIALS NETWORKS FOR BRAIN-INSPIRED INFORMATION PROCESSING

Crossbar array device architectures are currently well integrated in the semiconductor industry as they are the basis of random-access memory (RAM) designs. However, the process of fabrication of high density cross-bar arrays is elaborate and can require extreme ultraviolet (EUV) lithography, resulting in a costly and complex process. For example, Intel's Loihi 2 chip was fabricated using EUV lithography through the Intel 4 process (previously known as the 7 nm process).[10,65] Many lab-scale memristive devices also apply the crossbar array structure; with the most recent example the 256 x 256 memristor array reported by Rao et al., showing 2048 reachable conductance levels.[66] In order to prevent large scale leakage and interference between different nodes in the array, additional circuit elements are required, every node (memristor or resistor) needs to be accompanied by a transistor (1T1R architecture).[3,67]

While the highly ordered and well-defined layout of crossbar arrays allows for easy control and programming of the device operation, a disadvantage of the crossbar array is the limited connectivity between the nodes. Multiple crossbar layers should be stacked in order to approach brain-like connectivity, requiring complex circuit designs.[68] *We think it is the right time to take on a new challenge in neuromorphic hardware design, where we take advantage of the complexity of materials that consist of nanoscale networks with pre-designed characteristics that can potentially enhance the neuromorphic properties of the networks.*

The formation of networks is prevalent in nature, with one of the most profound examples being the neural network in our brains. Such networks are disordered and show a large degree of connectivity (e.g., 1 neuron connects to more than 1000 other neurons), in comparison to the well-defined crossbar arrays. The large connectivity of the brain network endows it with emergent behaviour and there are reports proposing that the brain may operate at the edge of criticality - a dynamical state between order (or synchronization) and chaos. While the exact driving force for criticality in the brain is unknown, one of the parameters that is thought to play a role is the branching factor of neurons, which is, essentially, an indication of connectivity.[69]

Recent computational studies have shown that a network of memristors acts as a memristor itself, showing increased tunability with respect to single devices.[70,71] This indicates that the extent of the hysteresis and the on/off ratio of the response of the network could be controlled by the organization of the network. Therefore, it is worth to look into dense self-assembled network structures and morphologies. In nature, self-assembly occurs as a way to minimize potential energy and the resulting complex interactions are difficult to engineer *via* a top-down approach. By taking advantage of self-assembly, efficient network structures can be found. These networks can be created at the nanoscale and increased connectivity could be achieved with respect to the traditional crossbar-array structure.

In the past decade, a few groups have been working in this direction, using network structures as neuromorphic materials; for example, networks of nanowires (NWs),[72–81] aggregations of nanoparticles (NPs),[82–93] or even networks of topological defects that originate during the formation of the material, such as domain wall networks in thin film metal oxides, that have recently been reported to form connected networks (Figure 1.3).[94] All of these examples are, in some way, self-assembled. Nanowire and nanoparticle networks work on the principle of forming electrical connections between conducting NWs or NPs that come in contact with each other upon being randomly deposited on a substrate through solution deposition or physical deposition techniques, such as sputtering. Nanowire networks often operate on the principle of core-shell structures, where the conductive NWs are at the core and are surrounded by a thin shell that stabilizes the NW; this can be an organic layer in the case of silver NWs, or a thin oxide layer in the case of for example nickel NWs.[72,77,78,81] Network connections, and memristive properties, arise from the formation of ionic filaments through the core-shell structure and allow for the creation of conductive pathways through the network. In the case of the NP networks, (metallic) inorganic NPs (Au, Sn, etc.) are typically deposited by sputtering. The surface coverage is monitored during deposition (by measuring the electrical resistance of the NP clusters in-situ) and the deposition is halted when percolation is reached.[82,84] A network is obtained through connections between different NP clusters as a result of the formation of conductive atomic bridges, or atomic switches, either through filament formation, or tunneling.[82,88,89] Both the NP and NW networks have shown memristive behavior and interesting network switching dynamics, such as winner-takes-all behavior, and have shown the ability to be applied for reservoir computing.[77,78,81,92,95] Reservoir computing uses a type of *so-called* Recurrent Neural Networks (RNN) that does not require to address all the different synapses in the network and can use the properties of dynamical, non-linear physical systems for some types of information processing.[96]

In the case of domain wall (DW) networks, the DWs are formed as an intrinsic property of the material in order to comply with the electric and elastic boundary conditions imposed by the (ferroelectric or ferromagnetic) domains within the thin films, the substrate strain, screening length of the electrode, etc.[97,98] For some materials, for example ferroelectric perovskites such as $BiFeO_3$ (BFO),[94,99–102] $BaTiO_3$ (BTO),[103] $PbZr_xTi_{1-x}O_3$ (PZT),[104–107] $LiNbO_3$,[108,109] the nonlinear optical material $KTiOPO_4$,[110] and hexagonal rare earth manganites such as $TbMnO_3$ and $ErMnO_3$,[111–114] the DWs are more conductive than the domains themselves, resulting in a network structure of conducting DWs that exists through the entire film, which in the case of the thin films can be very dense. Some of these DWs were shown to present memristive properties,[100,110] making them interesting for inherent-network brain-inspired

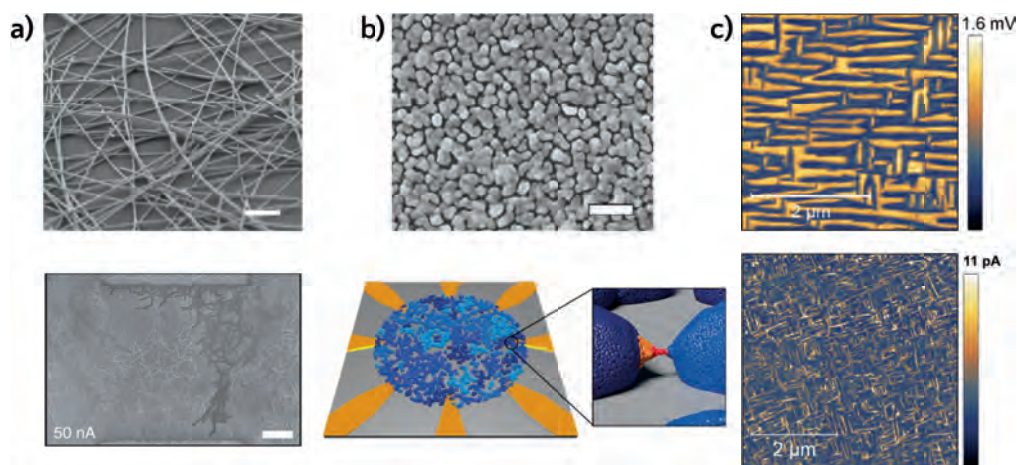

Figure 1.3 | a) Network of Silver nanowires (NWs) (top) and a visualization of winner-takes-all conduction in Ag NW networks imaged by scanning electron microscopy at a voltage of 50 nA (bottom). Reprinted with permission from Milano et al., Nat. Mater, **21**, 195-202 (2022).[81] Copyright 2022 Springer Nature; and Manning et al., Nat. Commun, **9**, 3219 (2018).[77] Copyright 2018 Springer Nature. b) Sn nanoparticle (NP) network (top) and a schematic representation of connections between different NP clusters (bottom). Reprinted with permission from Mallinson et al., Sci. Adv., **5** (2019).[89] Copyright 2019 AAAS; and Heywood et al., Neuromorph. Comput. Eng., **2**, 024009 (2022)[92] Copyright 2022 IOP publishing. c) Piezoresponse force microscopy image of the ferroelectric/ferroelastic domains in a $BiFeO_3$ thin film (top) and a conductive AFM image of the domain wall (DW) network, where the DWs are more conductive than the domains (bottom). Reprinted with permission from Rieck et al., Adv. Intell. Syst., **5**, 2200292 (2023).[94] Copyright 2022 Wiley-VCH

materials.[94,97]

1.4. FOCUS AND OUTLINE OF THIS THESIS

Here we propose a general method to create network structures of a large variety of functional materials, independently of their intrinsic interactions and their inherent ability to form networks. Specifically, this is achieved by using block copolymer (BCP) templating, where different structures and morphologies can be obtained simply by tuning the BCP block weights, allowing for different morphologies and length scales.[115,116] Metallic ions can be selectively incorporated into the self-assembled structures when one of the block segments is hydrophilic, while the other one is hydrophobic, being the microphase separation of the two blocks the driving force for the self-assembly of BCPs (this topic is discussed more in-depth in Chapter 3.3).[115]

Initial reports of structures obtained through BCP templating were of metallic nano-lines (Au, Pt, Pd, etc.),[117–119] but due to the versatility of the BCPs and solvents that can be used, this technique is also applicable to the fabrication of metal oxide nanostructures.[120–126] However, the fabrication of complex oxides has not been investigated as much as the simple oxides,[127,128] with only one report reporting the use of chemical solution deposition (CSD).[128] Additionally, network connectivity is not inherently linked to BCP templating. As

mentioned before, many morphologies can be obtained by tuning the BCP properties, from these morphologies, the gyroid structure is a 3D network, while the lamellar phase will only be network-like when the lamella are curved and interconnected. Stacking multiple layers of the lamellar phase creates a 3D network, but this still lacks some control over the resulting structure.[129–131] With BCP templating, sub-10 and even sub-3 nm pitch for lamellar morphologies have already been reported, allowing for structures with high connectivity and at dimensions rivaling/comparable to high-end lithography techniques.[132–135]

In this work the aim is to create self-assembled networks of nanoscale memristive devices with the intention to increase the palette of memristive devices to richer, more complex, and more tunable materials. We achieve this through the combination of polymer imprinting and polymer templating to form networks of different (complex) metal oxides through a chemical solution deposition method. Here the imprinting steps provide an array of ordered stripes, on top of which a lamellar BCP self-assembles into a network structure. This allows for an added control-factor in the network fabrication through the imprinted stripes, which could serve for example as electrode contacting-points, while still maintaining tunability of the BCPs to allow for further control of the final network structure.

As discussed, BCP templating of inorganic materials started with work from Chai et al.[117,118] where metallic ions were templated in BCPs to form metallic nanolines on silicon substrates. While memristive behaviour has been shown for metallic networks (see Section 1.3), this work aims to extend that to memristive networks of metal oxides. Several memristive properties are already known for metal oxides (see Section 1.2), allowing for large variation in device operation. Additionally, while metallic networks require low voltages for conduction, which is an advantage for operation purposes, currents through the network can become high, resulting in high power through the circuit. Oxides show more variability in the voltages needed to switch between different resistance states. While they sometimes require larger voltages initially (wake-up or forming, in case of filamentary switching),[63] the advantage is that the current flowing through the device is generally much lower compared to the metallic network counterparts; leading to an overall lower power consumption of the networks. The advantage of networks obtained through the combination of polymer imprinting and templating over disordered NW or NP networks is that the morphology and interconnectivity of the network can be controlled in the imprinted and templated networks. This control could aid in obtaining and tuning plasticity through the network morphology. Additionally, due to the solution-processing fabrication steps, the fabrication method is silicon compatible, which is an added benefit for future integration with industry.

1.4.1. OUTLINE

This thesis is organized according to the following Chapters:

- **Chapter 1** serves as the general introduction to this thesis, providing the reader with the motivation and background for this project and a framework for the rest of the thesis. In this work we aim to create self-assembled networks of nanoscale memristive devices, with the intention to develop richer, more complex, and more tunable materials. We achieve this through the combination of polymer imprinting and polymer templating to form networks of different metal oxides.

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- **Chapter 2** describes the experimental methods and techniques in detail. Some experimental difficulties and problem-solving strategies are discussed. The theoretical background for the major characterization methods is also explained in this chapter, as well as the motivation for using these specific techniques.
- **Chapter 3** is a review on the state-of-the-art of polymer templating of multifunctional oxide nanostructures at the time when this work was started. This chapter gives an overview on how polymer templating offers an interesting alternative for the fabrication of metal oxide nanostructures compared with other traditional methods for the fabrication of thin film heterostructures, such as pulsed laser deposition (PLD) and chemical solution deposition (CSD). Templating using sequential infiltration synthesis (SIS) and CSD is discussed and pathways to obtain complex structures using multiblock copolymers is discussed. Finally, an outlook on the progression of the field and interesting directions to investigate are provided. This chapter is based on the published paper: Xu, Berg* et al., *J. Appl. Phys.* **128**, 190903 (2020).
- **Chapter 4** is the first research chapter. Here the fabrication and (extensive) characterization of $BiFeO_3$, $SrTiO_3$, HfO_2, and $La_{0.7}Ca_{03}MnO_3$ networks are discussed. The diverse materials that are reported show promise for future applications in adaptable electronics and show that a multitude of materials is in reach for the combined templating and imprinting method. This chapter is based on the published paper: Berg et al., *ACS Appl. Nano Mater.* **5**, 9, 13349–13360 (2022).
- **Chapter 5** discusses the synthesis and characterization of $La_{0.7}Sr_{0.3}MnO_3$ (LSMO) structures, offering a perspective on the potential use of the LSMO as memristive material. The critical thickness of LSMO for electrical conduction is discussed, as well as the effect of size reduction in both the in-plane and out-of-plane directions in the case of the metal oxide networks. From here, we reason that the critical thickness needs to be overcome in order to obtain materials and devices that can show conduction at room temperature. Different multilayer structures are discussed in this chapter and a preliminary characterization of their electrical properties is presented.
- **General Outlook.** This short chapter provides an outlook and discussion on the impact of this work and the next steps that should be taken in order to create a future for self-assembled networks in neuromorphic applications.

*J. Xu and A.I. Berg contributed equally to this work

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