Memristive Memory Enhancement by Device Miniaturization for Neuromorphic Computing

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The areal footprint of memristors is a key consideration in material-based neuromorphic computing and large-scale architecture integration. Electronic transport in the most widely investigated memristive devices is mediated by filaments, posing a challenge to their scalability in architecture implementation. Here, a compelling alternative memristive device is presented and it is demonstrated that areal downscaling leads to enhancement in the memristive memory window, while maintaining analog behavior, contrary to expectations. The device designs directly integrated on semiconducting Nb-doped SrTiO₃ (Nb:STO) allows leveraging electric field effects at edges, increasing the dynamic range in smaller devices. The findings are substantiated by studying the microscopic nature of switching using scanning transmission electron microscopy, in different resistive states, revealing an interfacial layer whose physical extent is influenced by applied electric fields. The ability of Nb:STO memristors to satisfy hardware and software requirements with downscaling, while significantly enhancing memristive functionalities, make them strong contenders for non-von-Neumann computing, beyond complementary metal–oxide–semiconductor.

1. Introduction

The growing demand for applications such as artificial intelligence and the Internet of Things has given rise to critical challenges in the storage and processing of big data using existing computational architectures.[1] The currently employed von Neumann architecture, using complementary metal–oxide–semiconductor (CMOS) hardware, suffers from limited transmission speed[2–4] due to a memory throughput bottleneck as well as energy inefficiency and limited scalability.[4–6] Moving away from CMOS technology, toward logic-in-memory chips would alleviate some of the above issues but requires us to massively rethink every aspect of computing.[7] The first step toward this is identifying novel materials and devices with suitable physical properties. Resistive switching devices, or memristors, are one such class of devices where the resistance can be switched between several states. Reported in different ionic materials, they are distinguished by the switching mechanism as either occurring through the material bulk between two electrodes or interface-type where switching takes place in a localized region underneath the area of the electrodes.[8] Their ability to co-locate memory and computation, and exhibit characteristics absent in digital computing makes them important for novel computing approaches. Given the robust way in which the human brain is able to process large amounts of data with remarkably low power, it is unsurprising that it serves as a source of inspiration to the development of computing beyond using CMOS. As the brain utilizes a vast network, downscaling memristive devices is a crucial area of research to develop large scale neuromorphic systems.

For this material-driven research, the areal footprint in unconventional computing architectures that seek to integrate in-memory computing devices such as memristors is a prime consideration. Considerable research has been devoted to this in the realm of non-volatile conventional filamentary devices. The challenges in their implementation in such novel architectures, besides the requirement for unfavorable electroforming processes, lie in their switching endurance.[9] and their efficacy to exhibit discernible analog resistance states. Memristive devices that exhibit more than two stable states also greatly enhance integration density because each device can store multiple data bits in an analog manner.

In valence change memristors, where switching originates from filaments, such behavior is observed in large areal dimensions but is lost when devices are downscaled and conduction is mediated by a single nanoscale filament causing an abrupt transition between the two resistance states.[10] Further, the effects of Joule heating on filaments are an important consideration as devices shrink; Joule heating can cause a wide distribution of switching voltages and endurance deterioration. These limitations in device stability, endurance, and associated enhanced power of operation are major roadblocks in...
the successful implementation of filamentary devices in large scale architectures.

Memristive devices have the potential to be integrated in large scale architectures, for which they should exhibit large memory windows, high endurance and low variability.\(^{[10]}\) Herein the areal switching mechanism is a strong contender. A model system in which this mechanism is dominant is Schottky contacts on Nb-doped SrTiO\(_3\) (Nb:STO), formed at the interface with a high work function metal. It is widely accepted that in these material systems it is not the bulk of the device, but an area close to the interface that is responsible for the switching, a more detailed discussion on the proposed mechanisms is presented in Section S3, Supporting Information.

Distinguishing Nb:STO from conventional semiconductors such as Si, widely used in conventional architectures, is its dielectric permittivity which is comparatively large (300) and is strongly dependent on electric field. This property extends the parameter space for designing functionality; electric fields can be used to tune the barrier height and width relevant for memristive device design. We have previously shown that such Schottky contacts form robust memristors, exhibiting non-linear transport and continuous conductance modulation\(^{[12]}\) and that their behavior can be described by a power-law which can be successfully implemented as a learning algorithm.\(^{[13]}\) However, for the applicability of Nb:STO-based memristors as hardware elements for non-von Neumann computing architecture beyond CMOS, the focus should be on establishing their memristive performance with device miniaturization, which has not been shown on such semiconducting platforms. In this work, we demonstrate that memristive devices of Co Schottky contacts on Nb:STO exhibit an increase in the analog memristive memory window in devices down to 1 \(\mu\)m, contrary to expectations. Ionic defects are at the heart of memristive behavior, hence one of the following two scenarios is expected. For a homogeneous areal mechanism, the current density will scale with device area so that the device resistance in both the high resistance state (HRS) and the low resistance state (LRS) scales with the electrode size, but the ratio between them is area independent. Alternatively, the resistance window can be severely reduced or even vanish with downscaling due to insufficient ionic defects. However, we observe an enhancement in the memory window as the device area is reduced, with minimal device-to-device variation, an unforeseen finding.

To understand the microscopic nature of the switching, we conducted scanning transmission electron microscopy (STEM) on virgin samples and on samples subjected to either a positive (SET) or negative (RESET) voltage. Using integrated differential phase contrast (iDPC) we image oxygen atomic columns next to the heavy metal atomic columns. Virgin samples show the existence of a layer near the interface with neither the perovskite structure of the substrate nor that of the Co electrode. Applying a bias across the interface results in oxygen vacancy movement, which is a key factor controlling the resistance states. These new revelations are consolidated with a mathematical model describing the kinetics of trapping and de-trapping in dielectric materials and relates experimental results to the effective trapping density. Surprisingly, this is found to be larger for smaller junctions, suggesting that an increase in the density of traps is responsible for the increased resistance ratio and attributed to inhomogeneous distribution of the electric field due to device edges.

These memristive devices, integrated directly on a semiconducting platform, demonstrate multistate analog switching with remarkably high memory windows with downscaling, as well as high endurance and low device and cycle variation down to the smallest devices. Their ability to meet both hardware and software requirements for unconventional computing, make Nb:STO memristors strong material contenders for physical computing beyond CMOS.

2. Results

2.1. Electrical Characterization

Figure 1a shows a schematic of the device structure used for the electrical measurements. An array of circular Co electrodes of varying sizes are fabricated on a semiconducting Nb:STO single crystalline substrate. The bottom of the substrate serves as a back contact for the devices. The top electrodes were

Figure 1. State stability and multilevel memristive operation. a) Schematic of the fabricated devices on Nb:STO, electrical connections. Black lines are used to represent the varying overall electric fields acting over each area. The field strengths at the interface are also indicated by a color gradient, showing the fields are weakest in the central area (blue) and strongest around the perimeter (red). b) Current read at +0.3 V for device sizes of 100 \(\mu\)m (black), 10 \(\mu\)m (blue), and 1 \(\mu\)m (red). c) Current read at 0.3 V after switching between a SET voltage of +1 V (black, red and blue) or +2 V (green, purple, and orange) and a RESET voltage of -2 V (black and green), -2.5 V (red and purple), or -3 V (blue and orange). Each combination was repeated over 100 cycles.
patterned by a two-step electron lithography process using aluminum oxide as an insulation layer to define the contact areas and to prevent electronic cross talk. After fabrication, we performed small range voltage sweeps to characterize the virgin states of each device on a chip. The results for devices with radial dimension from 100 $\mu$m to 800 nm are shown in Figure 2, where each sweep followed a voltage sequence from 0 to $+1$ to $-1$ V and back to 0 V. We show four devices of each area, which are plotted in Figure 2a–f.

The current magnitudes for different devices of the same area show no significant differences down to 1 $\mu$m, indicating device-to-device variations are minimal. Establishing this is important as this signifies the sole influence of device area in determining the resistance ratio and rules out contributions from device-to-device variation. The 800 nm devices show a greater degree of variation; this is likely due to small differences in their areas and edges arising from the fabrication process and not inherent to the material or due to device fallibility. No significant differences in the current densities at low bias values are found in the virgin state, confirming that the entire device area contributes to the charge transport (Figure S1, Supporting Information). For all the devices, the current gradually increases and exhibits a small hysteretic effect from the virgin state, indicating that no forming step is required.

Figure 3a–f shows 1000 consecutive current–voltage ($I$–$V$) sweeps of these devices. Starting from a SET voltage of $+2$ V, each device is in an LRS, represented by the upper branches. After reaching the RESET voltage of $-3$ V and sweeping back, the devices are switched to an HRS (represented by the lower branches). In all device areas both the SET and RESET operation remain continuous, indicating the resistive switching retains its analog nature when downscaling. The cycling endurance was measured for over $10^5$ switching cycles without device failure, illustrating an endurance of $>10^5$. The current in the HRSs scales approximately with area at low bias values, while the low resistance current, is less closely correlated to the area. As a result, the resistance window increases with decreasing device area in both forward and reverse bias. Figure 1b and Figure S2, Supporting Information show the current and current density at a low read voltage of 0.3 V, respectively. Minimal cycle-to-cycle variations at low reading voltages are found with reproducible switching between clearly distinguishable states without degradation in device performance. This also establishes the low power operation of these devices after downscaling, which is important for memristor operation. As shown in Figure S3, Supporting Information, the device-to-device variation remains low down to 1 $\mu$m. The variation in the resistance ratio in the 800 nm devices is larger (Figure S4, Supporting Information), and will be discussed later.

The SET and RESET transitions are gradual and highly tunable. To demonstrate this, a 1 $\mu$m device was subjected to voltage sweeps varying between different positive (SET) and negative (RESET) voltages. Figure 1c shows that a wide range of stable states is available at a low read voltage of $+0.3$ V. The wide dynamic range combined with the large number of distinct addressable states ensures device reliability and increased memory storage capabilities. Each state maintains a narrow distribution of current values over the 100 cycles shown, reiterating the stability of the switching process.
2.2. STEM

A microscopy study of the Schottky interface was carried out using STEM. Figure 4 shows atomic resolution cross-section STEM-iDPC images of the Co/Nb:STO interface for samples in the unbiased virgin condition (Figure 4a), the LRS state (Figure 4b) and the HRS state (Figure 4c). To image lighter oxygen atoms, integrated into a matrix with heavier Sr and Ti atoms, we utilized STEM-iDPC instead of the more commonly employed STEM-high-angle annular dark-field (HAADF) imaging technique.[14,15] The STEM images in Figure 4a show that, apart from a thin interfacial region, the bulk STO consists of a cubic perovskite lattice and no defects are observable. All images taken within the bulk did not show any dislocation and possessed the expected perovskite structure as shown in Figure 4d. However, the structure close to the interface deviates from this perovskite structure and is deficient in oxygen. The migration of oxygen ions near the interface toward Co causes positively charged Ti ions to be displaced so that they no longer sit equidistantly from the Sr ions along <001>. Figure 4e illustrates how the loss of O ions gives rise to Ti displacements along the <001> direction away from the interface as well as along <110> (see Figure S7, Supporting Information) and is similar to what was reported in ref. [16] in La0.6Sr0.33MnO3/Hf0.5Zr0.5O2. We believe the creation of this thin layer to be related to the formation of a Schottky barrier. The analysis for a non-memristive interface with Ti contacts can be found in Figure S6, Supporting Information.

Figure 4b shows analogous results to Figure 4a, but now for the sample switched to the LRS, representing the upper branch in Figure 3, after the application of a positive bias voltage of 2 V. Comparing the two figures shows that in the LRS state the extent of the interfacial layer has decreased. This suggests that under the influence of a positive voltage, the labile bonds between Ti and interfacial Co atoms are broken and oxygen moves back into the STO substrate. A negative bias voltage of −3 V (corresponding to the lower branch in Figure 3), on the other hand, causes oxygen to move from STO to cobalt causing the formation of CoO and more oxygen vacancies in the STO, highlighted by a larger region over which Ti ions are displaced (see Figure 4c). This indicates that the formation of the CoO switches the sample to the HRS state. It has been shown[17,18] that the oxygen vacancy distribution inside the system will determine how the oxygen vacancies are affected by the applied voltage. The formation of an oxygen deficient interfacial layer confirms that in these samples the oxygen vacancies are concentrated near the interface. In this case, it is expected that the application of a positive voltage will cause oxygen vacancies to be repelled from the interface while a negative voltage will cause oxygen vacancies to be attracted to the interface, consistent with our findings. After removing the voltage, the interfacial layer did not reform over time, suggesting the presence of an oxygen-migration blocking layer. These results are summarized in Figure 4f.

Our results directly confirm the existence of a homogeneous oxygen deficient layer at the interface. The homogeneous nature of the defect state layer ensures ionic defects are retained with downscaling. We furthermore show that the physical extent of
the layer is reduced or extended when a positive or negative voltage is applied respectively. Although the uniform nature of the ionic contribution to switching is now verified, this does not explain the origin of the unexpected enhancement of the resistance window with downscaling. This we discuss next by considering the trapping of electronic charges at oxygen vacancy sites.

2.3. Model

In order to understand how the electrical properties of the devices are influenced by these oxygen vacancies, we consider the interaction between electrons and defect states. This interaction is most strongly evidenced by the retention characteristics, which have a slow decaying component. This behavior is caused by the detrapping of charges. It has been shown that this occurs over long timescales and the different states will remain clearly distinguishable for long time periods of hours and that the retention time is tunable by the applied stimuli.\(^{[12]}\)

We utilized short voltage pulses to measure the retention characteristics of each device in both an HRS and LRS. This was done by applying alternating SET and RESET pulses of +2 and −3 V respectively, and reading the small-signal current at either +0.3 or −0.5 V after each writing event. The state retention characteristics of the different devices are shown in Figure 5 for the LRS (red) and HRS (black). Over time, the current in both states tends to an intermediate value. For the LRS, the rate of change follows a power law that is commonly observed for charge trapping under bias in high-κ dielectrics, referred to as the Curie–von Schweidler law.

This law describes a non-Debye type relaxation in dielectrics. Empirical evidence of this behavior is seen in a wide variety of materials, but the precise physical origin remains unclear. Here we consider the effect of injected electrons becoming trapped in defects states within the dielectric. The space charge generated by these trapped electrons lowers the electric field, in turn reducing the flow of current through the dielectric.

In this case the trapping rate can be expressed as

\[
\frac{dn}{dt} = n_0 \sigma \frac{J_{th}}{q \nu_d} e^{-\frac{qV}{kT}}
\]

where \(n_0\) is the maximum number of traps available, \(J/q\) is the net flux density, \(\nu_{th}\) and \(\nu_d\) are the thermal and drift velocities respectively, and \(\sigma\) is capture cross-section. Solving this equation yields the following expression for \(n\)

\[
n = \frac{V}{kT} \ln \left( \frac{Q}{Q'} + 1 \right)
\]

where \(Q = \int J dt\) is the total injected charge and

\[
Q' = \frac{V \nu_d q}{n_0 k T \nu_{th} \sigma}
\]

Expressing the current as \(J = J_{th} e^{-\alpha}\) and extending this analysis results in

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**Figure 4.** Visualization of oxygen vacancy migration using STEM. a–c) iDPC-STEM images of Co/Nb:STO samples in the virgin (unbiased) state (a), the LRS (b), and the HRS (c), highlighting the structure close and far from the interface. d,e) The perovskite unit cell of STO, showing Sr in green, O in dark red and Ti in light red, viewed along the <110> in the pristine state (d) and with oxygen vacancies (e). The deficiency of O causes Ti atoms to move away from the vacancies as shown by the arrows. f) A schematic representation of how the interfacial layer is affected by biasing.
\[
\frac{\alpha - 1}{\alpha} \ln(J_s) = m E_{\text{tr}} + n
\]

(4)

where \(m\) is a constant.

We can also directly relate the trapping rate to the current. \(Q_t\) represents the charge that is trapped when charge \(Q\) is injected into the dielectric. The ratio \(\frac{dQ_t}{dQ}\) is a function of current. The current can be written as

\[
J = J_s \left( \frac{1 - (\alpha + 1)^{-(1/(\alpha + 1))}}{t_0} \right) \propto e^{V_0/(k_B T)}
\]

(5)

where \(\alpha \geq 0\) and \(J_s\) depends on the transport mechanism. For conduction following an exponential relation

\[
J_s \propto e^{V_0/(k_B T)}
\]

(6)

Here, \(V_0\) is a constant. The full derivation is shown in Section S1 and Figure S8, Supporting Information, and is also extended to show that it holds for other transport mechanisms.

Equations (4) and (6) serve as a direct mathematical proof that the exponent \(\alpha\) in the power law is related to the effective trap density or capacity of the dielectric to trap electrons. This derivation is applicable to a wider range of systems, irrespective of the choice of dielectric material. In Table 1 we show the LRS exponents, \(\alpha\) for each device. Larger values

Table 1. Magnitude of exponents, \(\alpha\), extracted by fitting a power-law to the low resistance states in the graphs in Figure 5.

<table>
<thead>
<tr>
<th>Radius [(\mu\text{m})]</th>
<th>Read at +0.3 V</th>
<th>Read at -0.3 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>(\uparrow)</td>
<td>(\uparrow)</td>
</tr>
<tr>
<td>1</td>
<td>0.85 (\pm) 0.03</td>
<td>2.17 (\pm) 0.02</td>
</tr>
<tr>
<td>10</td>
<td>0.47 (\pm) 0.02</td>
<td>0.987 (\pm) 0.002</td>
</tr>
<tr>
<td>100</td>
<td>0.041 (\pm) 0.004</td>
<td>0.626 (\pm) 0.007</td>
</tr>
</tbody>
</table>
are observed for smaller devices indicating that the trap density is higher in the smallest device compared to the larger device.

3. Discussion

While this model provides a clear correlation between trapping density and device area, it does not give information about the traps; we implicitly take all traps to be of the same kind, while in reality, the nature of traps can vary greatly. The trapping rate can depend on the spatial location of the traps and new traps can be generated via defect migration. For a more precise picture of the mechanism, we need to consider a distribution of traps with respect to their location within the dielectric. Evidenced by the STEM study, oxygen vacancies are the most important class of trapping defects to consider. They are abundantly present in STO due to their low formation (0.51 eV\(^2\)) and migration (0.62 eV\(^2\)) enthalpies and their locations within the energy landscape are well documented.[21]

From the discussion above, it is clear that the energy landscape of these Schottky junctions is far more complex than is captured by the most commonly used models that are based solely on parameters of the individual materials forming the contact.[22,23] Transport through these junctions is usually described by the thermionic emission equation, which includes an ideality factor accounting for the deviating transport from this ideal diode equation. This model furthermore does not consider that the interfacial area is not spatially homogeneous and that in devices of finite areas the boundary of the device will be relevant. In particular, it is known that near the edges crowding of the field lines leads to an enhancement in the field strength which can decrease the barrier width.[24,25] This is supported by the results of the finite element simulations in Figures S11 and S12. Supporting Information, showing a significant enhancement in the electric field around the edge and when downsca ling. From the simulations it is evident that there is still a clear field gradient in the 1 µm devices, indicating that a further increase in ratio with downsca ling can be expected, and the areal field shows no apparent saturation till around 10 nm.

The observed enhancement is especially important in Nb:STO-based memristive devices as the dielectric constant of the substrate strongly depends on electric fields.[26,27] This will further alter the potential landscape of the Schottky interface in such memristive devices. In particular, the dielectric permittivity of Nb:STO rapidly decreases in the presence of large electric fields which results in a decrease in the effective Schottky barrier width as illustrated in Figure 5g. Consequently, a large reduction in the barrier width is expected to occur near the device edges (Figure 5h). It has also been shown that an electric field can modify the defect states and significantly affect trapping parameters.[28]

Given that the charge transport is governed by the potential landscape, this will hugely impact the measured current, pictured in Figure S1i. Tunneling through the barrier will be enhanced near the device edges leading to a larger current near the device perimeter. This will be especially important in the LRS where the interface is depleted of trapped charges and the Schottky barrier is narrower, leading to more tunneling.[12,29]

Transport across the interface is comprised of thermionic emission and tunneling. The thermionic current density is expected to be independent of area and is the dominant mechanism in the HRS at low bias voltages, giving rise to the decreasing current in the HRS around zero with downsca ling observed in Figure 3. At higher voltage values, however, tunneling will also contribute to the current; the tunneling current density will increase with decreasing area. In Figure 1b, the current is read at +0.3 V where we expect both thermionic emission and tunneling to contribute to transport, giving rise to similar currents measured for the 10 and 1 µm devices in the HRS. The tunneling contribution increases in the LRS, especially in smaller devices due to the larger electric fields, resulting in the observed increase in current density with reducing area.

By applying a potential over the Schottky barrier, the Fermi level is shifted such that tunneling electrons sample different oxygen vacancy energy levels. As the reverse bias voltage is increased, electrons are gradually exposed to larger ranges of states in which they can become trapped. In addition, in reverse bias, the electric field at the interface becomes larger leading to a reduction in the dielectric constant and a corresponding decrease of the Schottky barrier widths. This decrease in width will be more pronounced in regions closer to the edge due to the local field enhancement. As a result of the narrower barrier, electron–electron scattering will be reduced and the trap states will act as the main barrier for transport. The stronger edge field may additionally facilitate the migration of oxygen vacancies resulting in a higher number of vacancies accumulating around the perimeter. Consequently, the trapping efficiency will be greater near the edge than in the center. This is a unique effect enabled by the electric field control of the dielectric permittivity, does not occur in conventional semiconductors and is relevant for Nb:STO memristive device design.

We can express the area and perimeter of a device with radius \( r \) as \( A = \pi r^2 \) and \( p = 2\pi r \) respectively. The ratio of the perimeter to area

\[
\frac{p}{A} = \frac{2r}{\pi r} = \frac{2}{\pi}
\]

indicates that the edge effects become more dominant as the device area is reduced. As a result, current flow at the perimeter will constitute a larger percentage to the overall transport behavior in smaller devices. This explains the enhanced current densities observed when downsca ling after applying large bias voltages as well as the larger effective trapping densities for smaller devices. Specifically, this field enhancement around the device edges gives rise to an increase in the dynamic range in smaller devices, and explains the unexpected resistance window scaling.

4. Conclusions

As a first demonstration of exploiting edge effect related additional electric fields, our work successfully demonstrates the ability to increase the resistance window by device miniaturization of interface memristors from 100 down to 1 µm, contrary to expectations, with exceptional robustness to device-to-device
and cycle variability. STEM images taken in the virgin, high, and low resistance states prove the existence of a homogeneous interfacial layer, deficient in oxygen, whose physical extent is influenced by applying an electric field. This, however, does not explain the enhancement in the resistance window with device downscaling. A model describing the interaction of electrons with oxygen vacancy trap states shows an increase in the effective trapping density with downscaling. The advantage of direct integration of devices on a semiconducting platform of Nb:STO allows for the locally enhanced fields to controllably tune the interfacial energy landscape at the interface, leading to a greater contribution of edge effects in smaller devices as confirmed by finite element simulations. With rapid advances made in the palette of materials and devices available for neuromorphic hardware, the thrust now should be in their efficient integration on semiconducting platforms for on-chip applications with substantial reduction in areal footprint. In this, our work provides an encouraging direction.

5. Experimental Section

Electrical Device Fabrication: A series of Co/Nb:STO devices were investigated, where the device area was varied across the series over a range spanning five orders of magnitude ranging from $10^{-12}$ to $10^{-8}$ m$^2$, with radii between 800 nm and 100 µm. The devices were fabricated using Nb:STO (001) substrates with a doping concentration of 0.1 wt% from Crystec. STO consists of alternating SrO and TiO$_2$ planes along the [001] direction. The as-received substrates have a slight miscut from the exact crystallographic direction and as a result, a mixture of both terminations exists at the surface. It has been shown that the local properties of Schottky barriers grown on the different terminations may differ, hence to minimize the variation of different areas on the substrate a single termination is desired. To ensure that the terminating layer is TiO$_2$, a chemical treatment was carried out with buffered hydrofluoric acid (BHF). A further annealing treatment at 960 °C in an O$_2$ flow of 300 cc min$^{-1}$ to facilitate the reorientation of surface atoms to form an atomically flat and straight terraced surface. Atomic force microscopy images were taken at different parts of the substrate and confirmed the existence of uniform terraces. The substrate was then coated with a negative resist (AZ nLOF 2020) and using electron beam lithography circles of different areas were patterned. A thick insulation layer of Al$_2$O$_3$ was deposited using electron beam vaporization and lift-off was carried out to define a set of direct contacts to the substrate. By means of a second lithography step with a positive resist (950k poly(methyl methacrylate)), square contact pads were defined, each covering a hole and part of the surrounding Al$_2$O$_3$: the dimensions of these pads were identical for each device to minimize spurious effects arising from significantly different contact resistances. Co (20 nm) and a capping layer of Au (100 nm) were then deposited using electron beam evaporation in high vacuum ($\approx 10^{-6}$ Torr).

Electrical Characterization: Electrical measurements were conducted using probes connected to two remote-sense and switch units of a Keysight B1500A Semiconductor Device Parameter Analyzer. During the voltage sweeping measurements, conducted using a sweeping measurement unit (SMU), the bottom of the substrate was held at 0 V while a voltage was applied to the top electrode. Due to the dodec nature of the devices in conjunction with large degrees of resistive switching, the measured currents during a single sweeping measurement spanned up to 9 orders of magnitude. For this reason, the measurements were performed using auto range for the measured current. The effects of this can be observed in the endurance cycling measurements which were performed at high sweeping rates in the form of plateaus in the current whenever a limit of the SMU range was reached.

STEM: The samples discussed in this work use STO (001) substrates with an Nb-doping in place of Ti of 0.1 wt% from Crystec. The surface was prepared using a chemical treatment with BHF. Next, the substrates were annealed at 960 °C in an O$_2$ flow of 300 cc min$^{-1}$. For STEM samples films were deposited by electron beam evaporation of 20 nm of Co capped with 20 nm of Au and 20 nm of Pt. From this, three types of STEM lamellae were prepared: virgin (unbiased) samples, LRS samples, and HRS samples. Using a probe station, samples were subjected to bias values of +2 V and −3 V to prepare samples in the LRS and HRS respectively. STEM lamellae were extracted from samples along the [110] direction using a Helios G4 CX dual beam system with a Ga focused ion beam. The lamellae were then thinned to make them transparent to electron using the focused ion beam. Imaging was carried out using a Thermo Fisher Scientific Temems Z SSTEM system operating at 300 kV.

STEM-HAADF images were most widely used, because they are readily interpretable with atomic columns being bright spots in a dark surrounding, where the brightness of the spots scale with the average atomic number $Z$ ($\propto Z^{1.7}$). This technique was well suited to image heavy elements, but lighter elements, such as oxygen, were harder to detect, and cannot be detected properly when integrated in a matrix with much heavier elements (like Sr). Therefore, to gain more insight into the important role played by the oxygen ions, STEM-IDPC was utilized here instead of STEM-HAADF imaging. This technique uses a power-law equation of the form $I = I_0(t - t_0)^{-\alpha}$ by means of the Levenberg-Marquardt algorithm; the reported errors were the standard errors calculated by this method. The fits are shown in Figure S9, Supporting Information. The inverse scaling of the exponent and device area was verified for different devices and different reading and SET voltages. Plotting and analysis of electrical measurements was done using OriginPro 8.5. Measurements were repeated on four devices of each area to check reproducibility and validity of results.

For STEM images, multiple regions for each one of the three bias conditions were taken to verify the results. The IDPC images were filtered by applying a high-pass Gaussian filter using Velox. Finite element modeling of the electric field profile at the interface was carried out using COMSOL Multiphysics.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.
Author Contributions
A.G. and T.B. conceived the idea and designed the devices. A.G. and D.G. fabricated devices for electrical measurements and performed electrical measurements, along with I.B. D.G. derived the mathematical model discussed in the manuscript. M.A. and A.G. fabricated lamalae for STEM and M.A. took STEM images. All authors analyzed the data, discussed the results, and agreed on their implications. All authors contributed to the preparation of the manuscript.

Data Availability Statement
The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords
areal scaling, beyond complementary metal–oxide–semiconductor, interface memristor, neuromorphic computing, scanning transmission electron microscopy

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