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## Charge transport and trap states in lead sulfide quantum dot field-effect transistors

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# Summary

Electronic devices nowadays have become an integral part of our day-to-day needs. Their great advancement has given remarkable impact in our lives, which covers many sectors including energy, healthcare, sensor, light industry, etc. To date, most of the electronic devices available in the markets are constructed from silicon and other highly crystalline semiconductors. These materials are mainly deposited using epitaxial growth method which requires ultra-high vacuum environment, high temperature, and energy intensive process resulting in high manufacturing cost.

In the past few years, colloidal quantum dots (QDs) have emerged as promising future semiconducting building blocks for electronic devices. These materials can potentially compete with epitaxial-based semiconductors as they can be processed by solution methods, which are compatible with low temperature processes and with device fabrication on plastic substrate. Thanks to the quantum confinement, their band gap is size-tunable ranging from ultraviolet to near-infrared, making them prospective candidates for well-controllable electronics and highly efficient optoelectronic devices. Among other types of QDs, lead sulfide (PbS) is one of the most promising because they can show strong quantum confinement in relatively large particle size (<20 nm). As the research on the PbS QD synthesis has been well developed, the size range can be achieved together with the precise control of shape, chemical composition, and surface properties.

QDs have a large surface to volume ratio, a typical characteristic of nano-objects. As a consequence, QDs have defect states on their surfaces which are responsible for charge carrier trapping within these materials. This charge trapping is one of main obstacles in further utilizing these materials for broad electronic and optoelectronic applications. For instance, in the application of field-effect transistors (FETs) based on PbS QDs, the charge transport is still limited. A problem further arises as some additional defects appear on the surface of gate insulators, one of main components in FET devices, lowering the carrier mobility in the fabricated devices. Several methods to improve the surface properties of insulators and to modify the properties of semiconducting films have been reported. These will be key strategies to understand and further improve charge transport in the FETs based on PbS QDs. The studies of these strategies are the focus of this thesis.

The surface properties of gate insulators are crucial in determining the electrical properties and the performance of FETs. In **chapter two**, we

introduced molecular dipoles on the surface of SiO<sub>2</sub> gate dielectric using self-assembled monolayers (SAMs). Using SAMs, the threshold voltages of the devices are shifted and show a linear relationship with the SAM doping concentration, providing an opportunity to tune the FET properties towards n-type or p-type depending on the used SAMs. The SAMs are also found to reduce the trap density in the devices, leading to the improvement of the electron mobility up to a factor of three.

The use of gate dielectrics with better surface properties together with comprehensive understanding on the nature of charge trapping in FETs is a necessary step to improve charge transport in PbS QD-FETs. In **chapter three**, we passivated the SiO<sub>2</sub> surface using hexamethyldisilazane (HMDS) and utilized hydroxyl-free Cytop dielectric. The HMDS treatment is found to improve the QD assembly organization and indeed passivate the dangling bonds on the SiO<sub>2</sub> surface, leading to the improvement of electron mobility by a factor of three. The use of Cytop gate dielectric further improves the mobility by one order of magnitude. Using a simulation, we showed that a significant decrease of the trap density of states (trap DOS) by almost two orders of magnitude is responsible for the improvement of the mobility in the devices.

In **chapter four**, we presented an analysis of the trap DOS in PbS QD-FETs utilizing several polymer gate dielectrics with a wide range of dielectric constants (2-41). We observed that the number of traps in the subthreshold regime increases with increasing the dielectric constant of the gate insulators. A consistent result was obtained from analysis using a computer simulation, where the increase and broadening of the trap DOS in the devices were observed with increasing the dielectric constant of the insulators. These results suggest the presence of increased disorder due to polaronic interaction at the semiconductor/insulator interface in PbS QD-FETs with increased dielectric polarization strength.

Doping is an effective tool to improve carrier mobility in semiconductors. In **chapter five**, we reported a strategy to heavily dope PbS QDs combining the use of benzyl viologen (BV) dopant with the engineering of the QD energy levels through the use of several capping ligands. With this doping, the electron mobility is improved by one order of magnitude. From the 4-terminal conductivity transistor measurement, the BV doping of the PbS QD films resulted in an electron mobility as high as 0.64 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> in devices employing SiO<sub>2</sub> gate dielectric.

The modulation of the inter-QD distances using mechanical strain is expected to determine the charge carrier transport in PbS QD-FETs. In **chapter six**, we demonstrated the effect of mechanical strain on the electrical properties of flexible ion gel-gated PbS QD-FETs. Using ion gel gating, a high electron mobility of 2.1 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> in the devices was achieved. The application of compressive strain results in the bending of the capping ligands and reduced

inter-QD distances, leading to the improvement of the mobility up to 45% ( $3 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ ) at 2% strain. Meanwhile, the oppositely applied strain leads to an increase of the inter-QD distances resulting in the reduction of the electron mobility in the devices. In addition, we also found that the compressive strain reduces the threshold voltage of the devices, which explains an efficient trap filling. Instead, the increase of the threshold voltage is observed with the application of tensile strain, which increases the carrier traps in the devices. Furthermore, we found that the tensile strain also results in the activation of the ligand chains, increasing the tunnelling barrier potential between QD solids.

To conclude, we investigated and improved charge transport in PbS QD-FETs by modifying the surface properties of gate insulators, doping of PbS QDs using organic molecules, and introducing mechanical strain on the devices. We demonstrated high mobility FETs based on PbS QDs, showing the importance of these materials as colloidal inks for future low cost and high performance plastic electronics.

