Charge transport and trap states in lead sulfide quantum dot field-effect transistors

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Chapter 4

Broadening of the Distribution of Trap States in PbS Quantum Dot Field-Effect Transistors with High-k Dielectrics

This chapter presents a quantitative analysis of the trap density of states (trap DOS) in PbS quantum dot field-effect transistors (QD-FETs), which utilize several polymer gate insulators with a wide range of dielectric constants. With increasing the dielectric constant of the gate insulators, the increase and the broadening of the trap DOS are observed which are attributed to the dipolar disorder and polaronic interactions appearing at strong dielectric polarization. Despite the increase of these polaron-induced traps, no negative effect is observed on the charge carrier mobility at the highest applied gate voltage. A proposed model related to the large electron-polaron separation distance explains the non-monotonic effect on the charge carrier mobility in high-k gated devices.

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4.1 Introduction

Reducing the operating voltage of FETs is a necessary step to use them for a broader range of applications. With conventional SiO_2 gate dielectric, the FET devices suffer from very high operating voltage due to a low gate dielectric capacitance, which is not compatible with practical applications. A lower operating voltage can be achieved through the use of gate insulators with high dielectric constant (high-*k*).[1–3] In organic semiconductor FETs, however, energetic disorder and polaron relaxation are enhanced at the semiconductor/insulator interface when utilizing high-*k* insulators ($k>3$).[4–6] This disorder and polaronic-related interaction may modify the electronic structure, such as the nature of trap states, at the semiconductor/insulator interface and are responsible for the reduced charge carrier mobility in some reported high-*k* gated organic FETs.[4] While the study on the localized (trap) states with the use of high-*k* insulators has been intensively done in organic FETs, only little information is available for FETs based on PbS QDs. Since the trap states can strongly determine the performance of QD-FET devices and at the same time dielectric insulators with higher-*k* are important in particular for low operating voltage, understanding the nature of trap states in PbS QD-FETs with increasing gate dielectric constant is crucial.

In this chapter, we present an analysis of the trap density of states (trap DOS) in PbS QD-FETs employing several polymer gate dielectrics. These solution-deposited polymer gate insulators display dielectric constants ranging from 2 to 41. Using these insulators, we first found that the number of deep traps extracted from the subthreshold swing of the devices increases with increasing the dielectric constant of the insulators. To understand this behavior, we quantified the distribution of the trap DOS versus energy in the devices by simulating the device working mechanism. In agreement to the subthreshold swing result, we observed the increase and broadening of the trap DOS with increasing the dielectric constant of the insulators. These results are rationalized in terms of an increased disorder due to polaronic interaction at the semiconductor/insulator interface in PbS QD-FETs with increased dielectric polarization strength.

4.2 Polarons at the semiconductor/insulator interface

When a gate voltage is applied on FET devices, charge carriers are accumulated in the semiconductor at the interface with the insulator. The microscopic nature of this interface has great influence on the accumulated charge carriers as well as on their transport. Sirringhaus et al., reported that dipolar disorder at the dielectric interface leads to the broadening of interface density of states (DOS) in polymer FETs.[5,6] This dipolar disorder originates from Fröhlich

polarons, which are caused by the interaction of the charges with induced dipole moments and polarization of the dielectric, as demonstrated in Figure 4.1 (a). With increasing the dielectric constant of gate insulators, strong polaronic interaction can be responsible for the increased disorder and carrier activation energy in FETs.[5,6] In agreement with this, Morpurgo et al., found that the polaron binding energy increases with increasing the dielectric constant of gate insulators.[4] These polaronic interaction and increased disorder also explain the origin of the reduced charge carrier mobility in some reported high-*k* gated organic semiconductor FETs.[4,6]

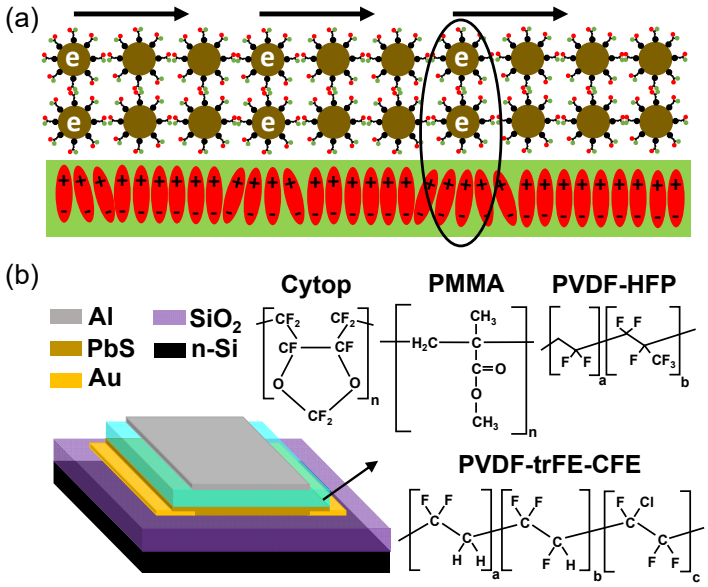

Figure 4.1 (a) Formation of polaron (black circle) due to the interaction between charges and dielectric polarization at the semiconductor/insulator interface. (b) Configuration of FETs with given chemical structures of polymer dielectrics.

To understand the nature of trap DOS in PbS QD-FETs with increased gate dielectric constant, a series of polymeric insulators with dielectric constant ranging from 2 till 41 were utilized. The polymer insulators were used in a bottom-contact top-gate structure of FETs as shown in Figure 4.1 (b). In addition, the used polymers are hydroxyl-group free, which allow excluding the effect of the interface traps due to dangling bonds on the dielectric surface. The interface traps given by these chemical groups have been known to influence the properties of the devices, as mentioned in the previous chapters, which may affect the analysis of results.[7] For this reason, we did not perform analysis on the charge accumulation using bottom SiO_2 gating. Furthermore, the bottom surface of the PbS films might have

different properties with respect to the top surface, which may influence our analysis.

4.3 PbS QD-FETs with polymer insulator gating

4.3.1 Characteristics of polymer insulators

As a first step to study the device properties, the characterization of the polymer insulator films including the film thickness (d) and the capacitance (C) was performed. The data of the film thickness and capacitance are presented in Table 4.1. The film thickness was characterized by using a Dektak Profilometer whereas the capacitance was measured by using Electrical Impedance Spectroscopy (EIS). To measure the film capacitance, a metal insulator metal (MIM) structure was used by sandwiching the polymer films with indium tin oxide (ITO)-coated glass substrates and thermally-evaporated thin aluminum (Al) layer. The dielectric constant (k) of the polymer insulator films was extracted using a standard parallel plate capacitor model. In Table 4.1, the terpolymer (PVDF-trFE-CFE) shows the highest dielectric constant among others with capacitance as high as 0.126 μF/cm^2, which enables to induce high carrier density in the devices.

Table 4.1 The characteristics of polymer insulator films.

Polymer	Thickness (nm)	Capacitance (nF/cm^2)	Dielectric constant
Cytop	650	2.7	2
PMMA	468	6.5	2.6
PVDF-HFP	308	26	10.5
PVDF-trFE-CFE	257	126	40.5

4.3.2 Electrical properties of FETs

The I_{ds}-V_g transfer characteristics in the linear and semi-logarithmic scale of the devices gated with different polymer insulators are shown in Figure 4.2. Generally, the devices show normally-off operation and good current modulation in the n-channel operation with on/off ratio of 10^4-10^5. In the p-channel operation, a small hole current is observed which indicates the ambipolarity of the devices. However, because of the weak hole current, the analysis on this study is focused on the n-channel operation of the devices. With increasing the dielectric constant of the polymer insulators, the on-current of the devices significantly increases. In addition, it is obvious that, with the use of high-k polymer insulators, the

operation voltage of the devices is reduced. The operation voltage can be further suppressed by optimizing the film thickness of the high-*k* insulators. Moreover, the devices show also some hysteresis in the transfer characteristics as shown in Figure 4.2. From the measurements, the devices employing high-*k* insulators show less hysteresis than those with low-*k* insulators (Cytop and PMMA).

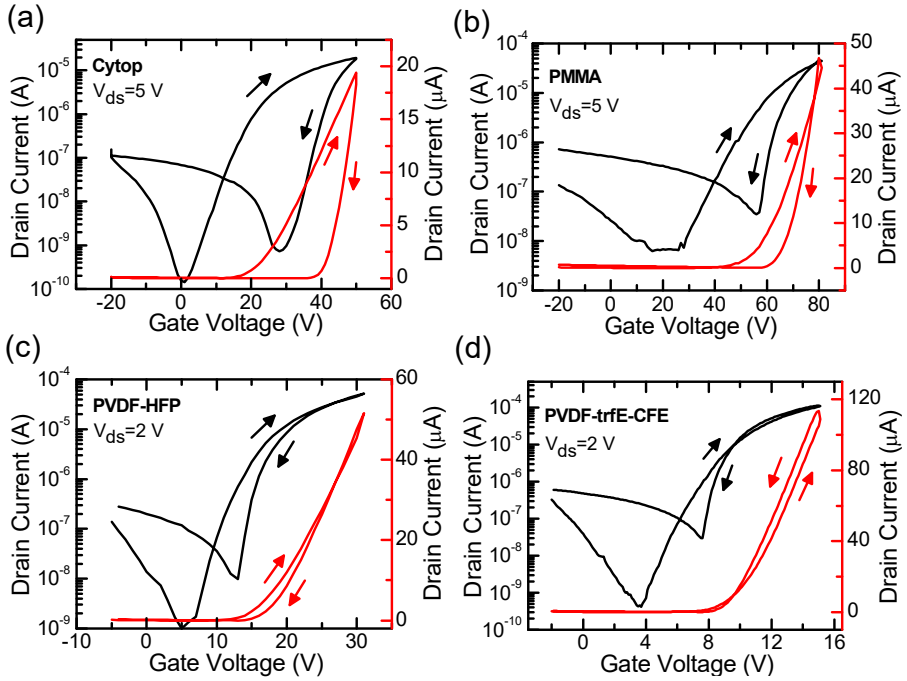

Figure 4.2 I_{ds}-V_g transfer characteristics of the devices with (a) Cytop, (b) PMMA, (c) PVDF-HFP, and (d) PVDF-trFE-CFE polymer gate dielectrics.

Table 4.2 Mobility and trap density in the devices with several gate insulators.

Polymer	Mobility ($cm^2V^{-1}s^{-1}$) similar n	high V_g	Trap density (10^{12} $cm^{-2}eV^{-1}$)
Cytop	0.12	0.12	1.3
PMMA	0.11	0.11	5.3
PVDF-HFP	0.09	0.14	9.2
PVDF-trFE-CFE	0.05	0.15	17

The average electron linear mobility in the devices using Cytop is 0.12 $cm^2V^{-1}s^{-1}$ at the highest applied gate voltage as given in Table 4.2. With this low-*k*

insulator, we are only able to accumulate charge carrier concentration up to 4.7 x 10^{11} cm^{-2}. By using high-*k* PVDF-trFE-CFE insulator, the carrier concentration can be improved by one order of magnitude (4.6 x 10^{12} cm^{-2}) at relatively low gate voltage (15 V). In PbS QDs, carrier traps mainly come from dangling bonds on the QD surfaces, which have strong influence on the charge carrier transport.[8–12] In contrast to organic semiconductor FETs, the increase of carrier density in PbS QD-FETs is expected to have great impact on charge carrier mobility particularly due to the filling of the surface traps.[13–15] However, no significant change in the charge carrier mobility is observed with this increased carrier density, as given in Table 4.2. Using PVDF-trFE-CFE insulator, the average mobility is estimated to be 0.15 $cm^2V^{-1}s^{-1}$ at maximum applied gate voltage, which is only a few percent higher than that measured with Cytop gating. Furthermore, a reduction in the carrier mobility with the high-*k* dielectrics is even observed when comparing the mobility values at similar carrier density (~4.2 x 10^{11} cm^{-2}). At this point, different phenomena are occurring when high-*k* dielectrics are used. The increase of interface disorder in the devices with high-*k* dielectric gating, which suppresses carrier transport, may be evoked.

4.4 Electronic structures of traps with high-*k*

4.4.1 Density of traps in subthreshold regime

To further investigate the reduced charge carrier mobility when comparing the devices at similar carrier density, the number of traps (N_{traps}) in the devices is estimated using the subthreshold swing formula as given in equation 1.14. From our measurements in Figure 4.2, it is obvious that the subthreshold swing decreases with increasing the gate dielectric constant as expected from,[16,17]

$$SS = \frac{k_B T \ln 10}{e}\left(1 + \frac{e^2 N_{traps}}{C_i}\right) \qquad (4.1)$$

where k_B, T, and e are *Boltzmann* constant, temperature, and elementary charge constant, respectively. However, if the subthreshold swing is analyzed in more detail, the actual values do not decrease as fast as we would expect when considering the effect only of the dielectric, meaning that an additional effect comes into play at higher dielectric permittivity. The only unknown parameter in equation (4.1) is the number of traps, which might increase due to an increase of the dielectric permittivity. Figure 4.3 presents the number of electron traps (N_{traps}) extracted from subthreshold regime using equation 1.14. It is obvious that the number of electron traps in the devices increases with increasing the dielectric constant of gate insulators. In the devices with Cytop gating, the number of electron traps is as low as 1.28 x 10^{12} $cm^{-2}eV^{-1}$, which is comparable to a previous

report.[7] At increased gate dielectric constant with the use of PVDF-trFE-CFE terpolymer, a significant increase in the electron traps by one order of magnitude (1.82 x 10^{13} $cm^{-2}eV^{-1}$) is observed. These increased carrier traps can explain the reduction in the mobility when comparing the mobility values at similar carrier density. In addition, this result can also be responsible for the mobility characteristics at maximum applied gate voltages with the high-*k* dielectrics. Furthermore, the increase of carrier traps and the mobility characteristics in the devices with the high-*k* dielectrics are an indication of the existence of polaronic-related interaction at the semiconductor/insulator interface, as observed in organic semiconductor FETs.[4–6]

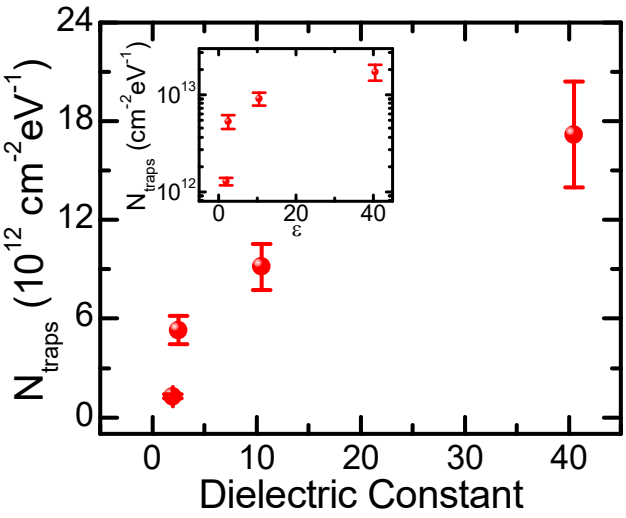

Figure 4.3 The number of electron traps in the devices as a function of dielectric constant extracted from subthreshold regime. The inset displays the number of traps in semi-logarithmic scale.

4.4.2 Distribution of trap DOS

To have further understanding on the nature of the trap DOS in the devices with increasing the dielectric constant of polymers, we performed a computer simulation on the I_{ds}-V_g transfer characteristics of the fabricated devices. The simulation is performed by solving the drift-diffusion and Poisson equation on the I_{ds}-V_g transfer characteristics of the devices following a numerical model developed by Oberhoff et al.[18] This simulator is based on general principles and can be applied to study a wide range of semiconducting materials. Although the subthreshold swing equation (4.1) can estimate the number of carrier traps in the devices, it can only quantify the traps at a certain energy level in the subthreshold

regime, whereas the simulation can analyze the number of traps in a broad energy range.[19–22] Furthermore, this simulation can explain the origin of a significant improvement of the charge carrier mobility in PbS QD-FETs with hydroxyl-free dielectric gating as previously mentioned in chapter 3.[7]

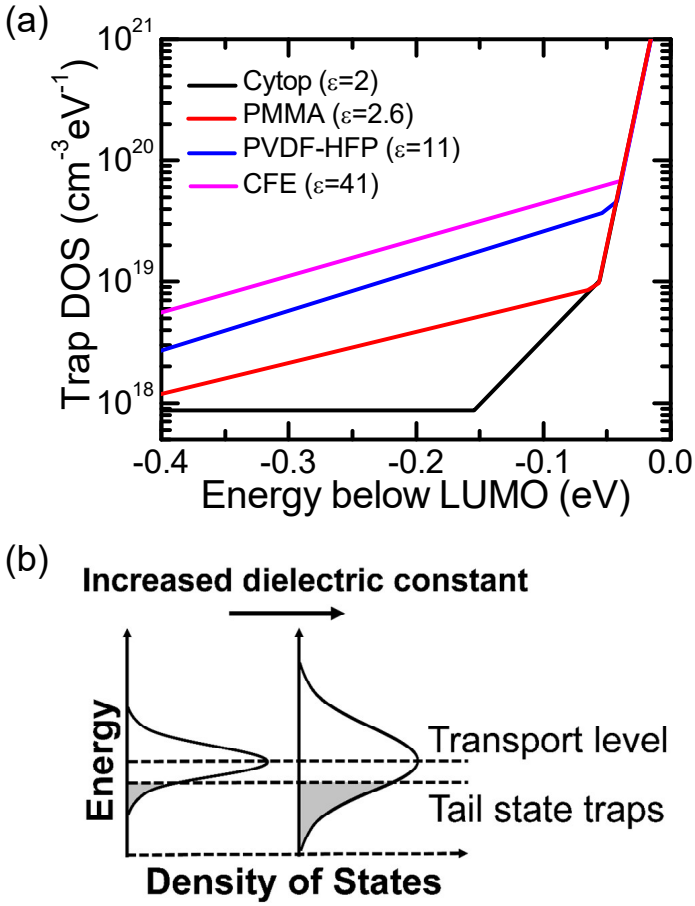

Figure 4.4 (a) Distribution of trap density of states (trap DOS) close to LUMO in the devices with different dielectric constants of gate insulators. (b) Schematic of broadening of tail trap states with increasing gate dielectric constant where the transport level corresponds to the LUMO of QDs.

Figure 4.4 (a) shows the analyzed density of trap states close to the LUMO level in the devices, fabricated with different polymer gate dielectrics. In agreement to the result in Figure 4.3, an increase of the carrier traps over a wide energy range close to the LUMO energy (electron traps) is also observed with increasing the dielectric constant of gate insulator. The analyzed density of trap

states is about 0.4 eV below the transport level (LUMO) of the charge carriers. As PbS QD-FET devices show slight ambipolar characteristics, the analysis of the traps is limited to this energy level to minimize the error due to the minority charge carriers (holes), which may exist close to the off-state of the devices. In addition to the increase of the trap DOS, the broadening of the trap DOS with increasing the gate dielectric constant is also observed as displayed in Figure 4.4 (a). The schematic of the broadening of the trap DOS with high-*k* dielectrics is shown in Figure 4.4 (b). The origin of the increase and of the broadening is most likely a consequence of the polaronic interaction at the semiconductor/dielectric interface which modifies the already-present disorder. This analysis is supported by the fact that the polaron relaxation has great impact on the density of states in polymer semiconductor FETs employing gate insulator with dielectric constant (k) > 3, as confirmed by charge-modulation spectroscopy (CMS).[5,6] These results confirm that the polaronic interaction at the semiconductor/insulator interface also has important effects on the behavior of PbS QD-FETs.

Finally, as we analyze the extracted mobility and the calculated trap DOS, the increase of charge trapping is expected to greatly suppress carrier transport, thus charge carrier mobility, in the devices. In line with this, the mobility decreases with increasing the dielectric constant of the gate insulators when we compare the mobility values at similar carrier density as displayed in Table 4.2. Meanwhile, at respective maximum applied gate voltages with different dielectrics, the mobility slightly increases with increasing the gate dielectric constant (see Table 4.2). In contrast to these results, the mobility in organic semiconductor FETs monotonically decreases with increasing the dielectric constant of gate insulators at all range of the applied gate voltages.[4] To understand these results, we propose that the interplay between charge trapping and trap filling process might take place in the devices. With increasing the dielectric constant of gate insulators, the increased carrier density is expected to fill the traps in the devices. Meanwhile, because the polaron-induced traps are increased at the same time, many gate-induced charge carriers are used to fill the trap states. Therefore, the effective free carriers with the high-*k* dielectrics will be only slightly higher than in the devices with Cytop, leading to a small improvement of the charge carrier mobility. Another possible explanation for the less affected charge carrier mobility than in organic transistors at high gate voltage is a large separation between polaron and the accumulated charge carriers in PbS QDs. In PbS QD-FETs, the top surface of the dielectrics is separated by the crosslinking EDT ligands which have length about 0.4 nm, while the radius of QDs is around 1.8 nm. As the accumulation of charge carriers in PbS QDs is assumed to be in the center of mass of the QDs, therefore, the total separation distance between polaron and the accumulated charge carriers is around 2.2 nm. Moreover, some residual oleic acid ligands on the bottom side of QDs may also exist which can increase the

separation distance. This larger polaron separation distance than in the case of polymer semiconductors (~0.3 nm) may minimize the effect of polaron on charge carrier mobility in our devices.[5,6] However, despite the large polaron separation distance, the trap states are still greatly influenced by the polaronic interaction. Nevertheless, the charge carrier mobility at all range of the applied gate voltages is expected to be greatly affected by the polaronic interaction at low temperature.

4.5 Conclusion

We have performed a study on the analysis of the trap DOS in PbS QD-FETs employing several high-*k* polymer gate insulators. With increasing the gate dielectric constant, we observed the increase of the electron traps in the devices as extracted from subthreshold regime. By using a computer simulation, we further analyzed the detailed distribution of trap DOS in the devices close to the LUMO level of PbS QDs. We found a general broadening of the trap DOS which is attributed to the increased disorder due to polaronic-related interactions at the semiconductor/dielectric interface. While the increased trap states effectively influence the mobility compared at similar carrier density, the extracted mobility at maximum applied gate voltages was not significantly affected by the polaronic interaction which is likely due to the interplay between trap filling and increased charge trapping as well as the large separation distance between polarons and free carriers in PbS QDs. Our results clearly show that by careful choice of dielectrics, PbS QD FETs with low operating voltage can be built without reducing the charge carrier mobility, which is a fundamental insight to further utilize colloidal QD systems in optoelectronic applications.

4.6 Methods

Device fabrication. The deposition of PbS semiconducting thin films was performed by spin-coating 10 mg/mL of oleic acid-capped PbS solution in chloroform on SiO_2/Si substrates. To improve the film conductivity, we exchanged the long oleic acid ligands with shorter molecules, namely 1,2 ethanedithiol (EDT). The concentration of the EDT solution was 1%v/v with acetonitrile as a solvent. The deposition of the PbS thin films, as well as, the ligand exchange, was performed using a layer-by-layer (LbL) spin-coating procedure. After each ligand exchange, pure acetonitrile was dropped on the films to remove unbound EDT and native oleic acid ligands. The PbS layer deposition and the ligand exchange were repeated for 5 times until desired thickness was reached. After the deposition, the devices were annealed at 120^{o}C for 20 min to remove residual solvent and to promote coupling between QDs, thus improving the conductivity without sintering the QDs. As gate dielectrics, we used four different polymer insulators

namely Cytop, polymethylmethacrylate (PMMA), polyvinylidene fluoride hexafluoro-propylene (PVDF-HFP), and polyvinylidene fluoride-trifluoroethylene-chlorofluoroethylene (PVDF-trFE-CFE). In this study, pure Cytop (CT-809M) was used without further dilution. PMMA was dissolved in ethyl acetate with concentration of 80 mg/mL. To prepare PVDF-HFP solutions, we dissolved the polymer in dimethylformamide (80 mg/mL). The last dielectric, PVDF-trFE-CFE, was dissolved in cyclohexanone to form a solution with concentration of 60 mg/mL. All these polymers, were used to vary the dielectric constant of the gate insulators in the devices in the range between 2 and 41. The deposition of the polymer insulators was done by using spin-coating on the previously-deposited active layer of PbS QDs. The devices were then annealed at 95^{o}C for 1 h to remove residual solvent. Finally, a thin layer of aluminum (50 nm) was evaporated as top gate electrode. All device fabrication was performed in an N_2-filled glove box.

FET electrical characteristic measurements. The electrical characteristics of FETs were measured using an electrical probe station (placed in an N_2-filled glove box) that is connected to an Agilent B1500A semiconductor parameter analyzer.

4.7 References

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