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Charge transport and trap states in lead sulfide quantum dot field-effect transistors

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Chapter 3

Dielectric Surface Passivation and Hydroxyl-free Polymer Gating in PbS Quantum Dot Field-Effect Transistors

In this chapter, the effect of gate dielectric surface passivation and hydroxyl-free Cytop polymer gating in PbS quantum dot field-effect transistors (QD-FETs) are studied. The passivation of the gate dielectric surface through the use of self-assembled monolayers (SAMs) results in a significant improvement of electron mobility due to reduced interface traps and improved particle assembly organization. With hydroxyl-free Cytop polymer gating, the charge carrier mobility in the devices is further improved by one order of magnitude. The calculation of the trap density of states (trap DOS) using a computer simulation shows that a significant reduction of the trap DOS over broad energy distribution is the origin of the improved charge carrier mobility in the devices.

M. I. Nugraha, R. Häusermann, S. Z. Bisri, H. Matsui, M. Sytnyk, W. Heiss, J. Takeya, M. A. Loi, *Adv. Mater.* **2015**, *27*, 2107

3.1 Introduction

The fabrication of field-effect transistors (FETs) is one of the best methods to evaluate charge transport properties in semiconductors, including QD assemblies.[1,2] Since FETs are interface-based devices, charge trapping is not only influenced by the properties of the active layer (the QD assembly) but also by the nature of the gate dielectric and its surface. Many efforts have been done to enhance the carrier mobility in PbS QD transistors. These attempts include variation of crosslinking ligands,[3–6] chemical post-deposition treatments to vary doping levels or to fill carrier traps,[7–9] increasing the chemical purity,[10] and controlling the effect of oxygen/moisture during fabrication.[4,5] Nevertheless, the typical mobility is still only up to 10^{-2} $cm^2V^{-1}s^{-1}$, with the exception of sintered PbS QDs, which however often give rise to unipolar devices with limited on/off ratio,[8,11] and the devices which utilize ionic-liquid gating that allows accumulating a higher carrier density than trap density.[4,12,13] In devices using conventional dielectrics such as SiO_2, the transport characteristics are still trap dominated.

In this chapter, we demonstrate a high electron mobility and a very low trap density in ambipolar PbS QD-FETs through the improvement of the QD assembly and the utilization of an amorphous fluoropolymer (Cytop) thin film as gate dielectric. Cytop is a hydroxyl-free and transparent polymer dielectric which has a dielectric constant of 2–2.3. We first improved the assembly organization of the 3-mercaptopropionicacid (3MPA) cross-linked PbS nanocrystals on the SiO_2 surface through the utilization of hexamethyldisilazane self-assembled monolayers (HMDS SAMs). This SAM treatment passivates the silanol on the SiO_2 surface that may act as electron trapping site. Cytop was deposited on top of the PbS nanocrystal assembly as second gate structure. The dual-gated FET structures using Cytop as a top gate and SiO_2 as bottom gate dielectric (Figure 3.1), were utilized to compare the influence of the two different dielectrics on the same PbS nanocrystal assembly. Finally, from the obtained transport characteristics, the simulation and numerical fitting to quantify the trap density of states (trap DOS), we observed for both holes and electrons in the FETs a sheet trap density lower than 10^{12} cm^{-2}, which explains the high electron mobility of 0.2 $cm^2V^{-1}s^{-1}$.

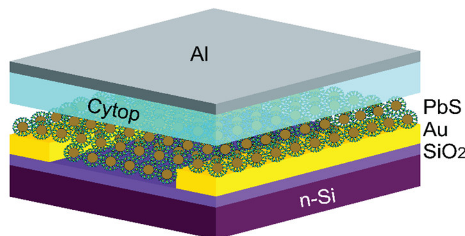

Figure 3.1 Configuration of PbS QD-FETs with SiO_2 bottom and Cytop top gate dielectrics.

3.2 Properties of PbS FETs with HMDS-treated SiO_2

3.2.1 Morphology of PbS films

The deposition of PbS QD films for FETs as well as for solar cells, is commonly performed using a layer-by-layer method to ensure effective ligand exchange. Therefore, the assembly organization of the first QD monolayer is the most crucial factor that determines the morphology of the successive layers. A conventional method for the deposition of QDs on a clean SiO_2, which has been used to successfully demonstrate well-performing devices,[4,5] produces clusters instead of large scale homogeneous films. The clustering is observed from the first monolayer after the ligand exchange of oleic acid with 3MPA as shown in Figure 3.2 (a). The formed clusters can be as thick as the equivalent of 3 monolayers, resulting in a root mean square (RMS) roughness of about 2.4 nm.

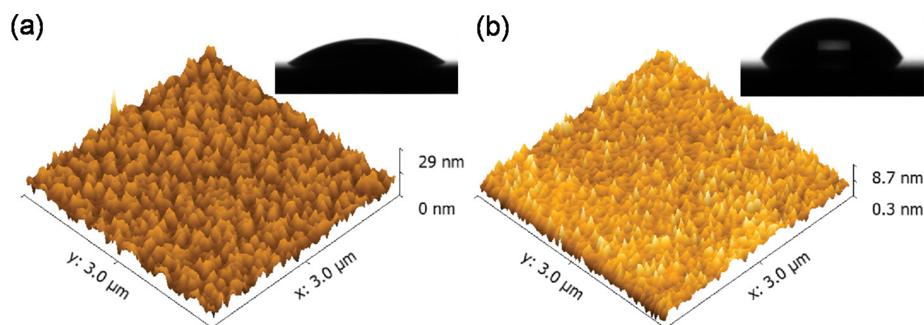

Figure 3.2 AFM images of (a) the first PbS QD layer on bare SiO_2 and (b) on HMDS-functionalized SiO_2. The inset shows the water contact angle of untreated and HMDS-treated SiO_2 surfaces.

To increase the hydrophobicity of the substrate, the SiO_2 surface was functionalized using hexamethyldisilazane self-assembled monolayers (HMDS SAMs). The HMDS-functionalized SiO_2 shows a water contact angle of 60°, which is increased significantly with respect to the contact angle measured for pristine SiO_2 (30°), indicated in Figure 3.2 (a) and (b). From the AFM micrographs, the surface of HMDS-treated SiO_2 is comparably smooth as that of the pristine SiO_2 as shown in Figure 3.3 (a) and (b). The smoothness of the surface and the high water contact angle clearly show that HMDS forms a well packed self-assembled monolayer and passivates the silanol (hydroxyl) groups on the SiO_2 surface. This functionalization significantly improves the assembly-order of the deposited PbS QDs. The RMS roughness of 0.8 nm indicates that no significant clustering observed in the first monolayer of the nanocrystal assembly after ligand exchange as displayed in Figure 3.2 (b). This indicates that the use of HMDS-SAMs

homogeneously reduces the surface energy for the deposition of PbS QDs from chloroform-based solutions.

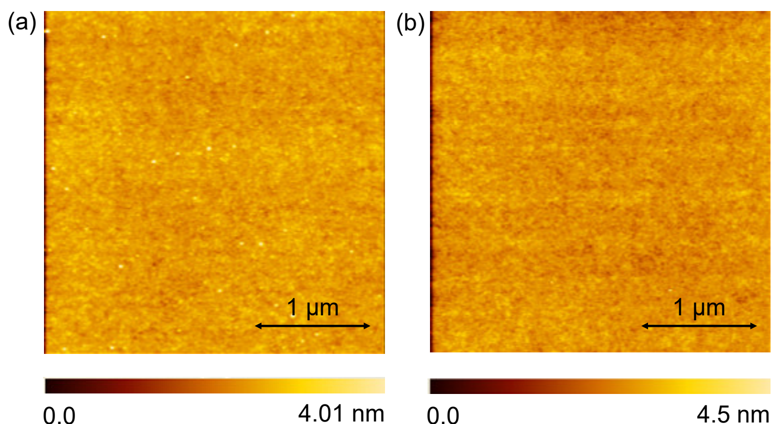

Figure 3.3 AFM images of (a) bare SiO_2 and (b) HMDS-treated SiO_2.

3.2.2 Electrical properties of PbS QD-FETs

PbS QD-FETs prepared on HMDS-treated SiO_2 were first operated as bottom-gate bottom-contact FETs with SiO_2 as gate dielectric. The configuration of the devices is displayed in Figure 3.1. The I_{ds}-V_{ds} output characteristics of the FETs with SiO_2 accumulation are shown in Figure 3.4 (a). The FETs show ambipolar properties with more electron-dominated characteristics, consistent with previous reports on PbS QD-FETs using 3MPA ligands.[4,5] Both, n- and p-channel output, show clear current saturation behaviors. In the small drain voltage operation, it is obvious that the devices exhibit nearly ohmic-like injection, both, for holes and electrons.

Figure 3.4 (b) shows the I_{ds}-V_g transfer characteristics of electron and hole modulations in the corresponding transistors. The electron on/off ratio achieves a value as high as 10^6. The fabricated devices have a 20 µm channel length and a 10 mm channel width, the capacitance of SiO_2 is 15 nF/cm^2. The maximum extracted mobility value in the linear regime is 0.07 cm^{2}V^{-1}s^{-1} for electrons and 5×10^{-5} cm^{2}V^{-1}s^{-1} for holes. The electron mobility is reasonably high for non-sintered ambipolar PbS QD-FETs that show high on/off ratio of 10^6 using SiO_2 gate dielectric and 3MPA ligands. The non-sintered PbS QD films are revealed from the absorbance spectrum that still maintain excitonic peak even after annealing the PbS films at 140°C as displayed in Figure 3.5.

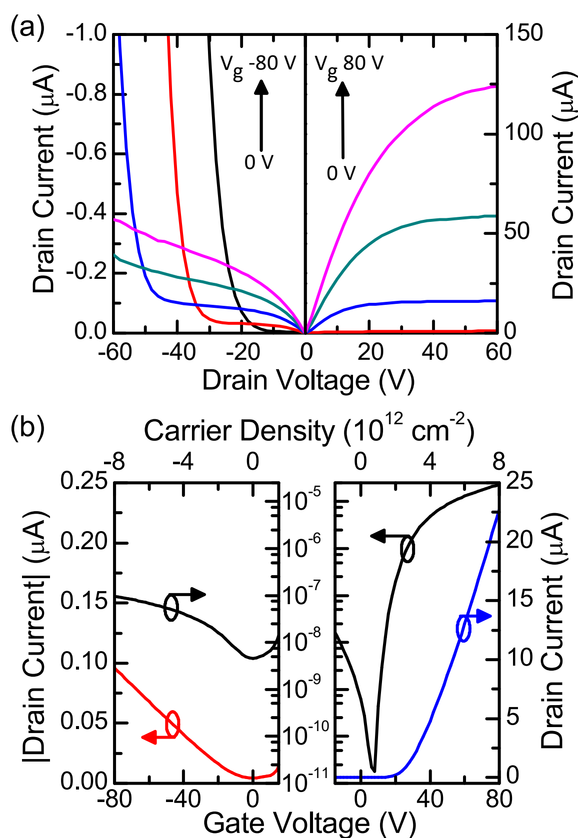

Figure 3.4 (a) I_{ds}-V_{ds} output and (b) I_{ds}-V_g transfer characteristics of PbS QD-FETs with HMDS-treated SiO_2. The applied V_{ds} in the transfer characteristics is ±5 V.

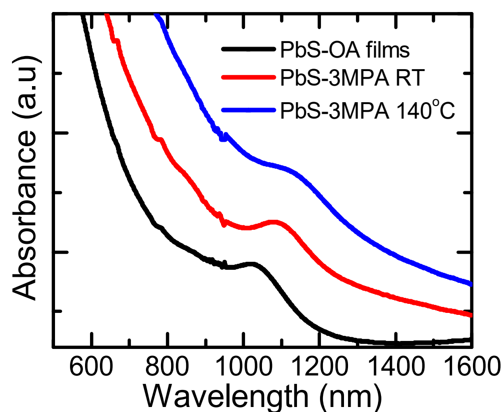

Figure 3.5 Absorbance spectrum of PbS QD films with oleic acid (black), 3MPA without annealing (red), and 3MPA ligands after annealing at 140°C (blue).

We compare the above-mentioned results with those from reference devices, in which the PbS layers were deposited on the top of bare SiO_2 (without HMDS treatment) and where the clustering of QDs occurs. From the parameters extracted from the device characteristics of the reference samples in Figure 3.6 (a), it can be deduced that the improvement of the QD assembly organization leads to an increase of the carrier mobility of about a factor of 3 for electrons. There is, however, no significant change in the hole accumulation. Two main differences can be observed from the comparison of the two types of devices. In the reference samples, the source-drain current in the n-channel saturation regime shown in Figure 3.6 (b) decreases with the increase of V_{ds}, which is not observed in the case of the HMDS-treated samples. This decrease of the current in the saturation regime can be attributed to the trapping of electrons.

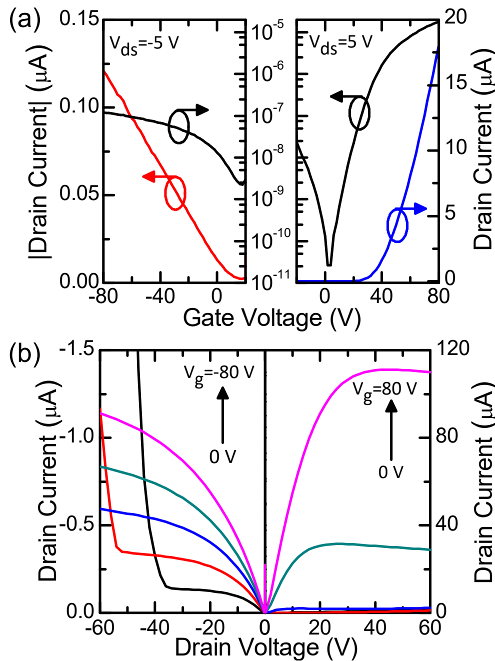

Figure 3.6 (a) The transfer and (b) output characteristics of PbS QD-FETs with bare SiO_2.

The nature of charge trapping in FET devices can also be estimated from the subthreshold swing in the transfer characteristics of the devices. Figure 3.7 (a) shows the comparison of the n-channel I_{ds}-V_g transfer characteristics between the HMDS-treated devices and the reference devices fabricated on bare SiO_2. Obviously, the devices with HMDS-treated SiO_2 show a lower subthreshold swing (SS = 2.71 $V.dec^{-1}$) than the reference devices (SS = 6.77 $V.dec^{-1}$). The lower subthreshold swing corresponds to a reduced interface trap density due to the passivation of silanol groups after HMDS treatment.

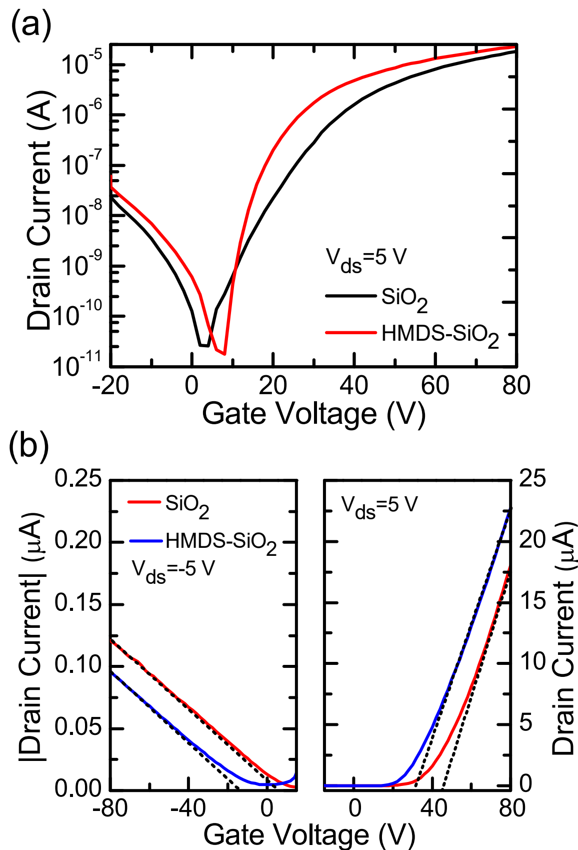

Figure 3.7 Comparison of the transfer characteristics in the devices with bare and HMDS-treated SiO_2 in (a) semi-logarithmic and (b) linear scale.

At this point, it is also interesting to investigate the effect of HMDS surface treatment on the doping behavior in the devices as indicated from the threshold voltage values. By using the intercept linear extrapolation of source-drain current to the gate voltage axis in the linear scale of transfer characteristics shown in Figure 3.7 (b), we obtained an average V_{th} for bare SiO_2 of 41.3 V and 12.6 V for electrons and holes, respectively. The devices that were treated with HMDS SAMs demonstrate an average threshold voltage of 27.2 V and -11 V for electrons and holes, respectively. This indicates that the HMDS SAM treatment shifts the electron threshold voltage as much as -14.1 V and the hole threshold voltage as much as -23.6 V. The transistors that undergo the HMDS treatment show electron doping, indicating less trapped electrons and the effect of the introduction of interface dipoles. The influence of the attached HMDS molecules on the SiO_2 surface dipole moment was then characterized using Gaussian program. After HMDS treatment, we found that the dipole moment on the SiO_2 surface was

changed by 0.61-0.98 D. It has been reported that the change of the dipole moment at the dielectric interface can influence the threshold voltage values.[14,15] The threshold voltage shift can be estimated from,[16,17]

$$\Delta V_{th} \approx -\frac{(C_s + C_{ox})t_s}{\varepsilon_o \varepsilon_d C_{ox} t_d A} \mu_{SAMs} \tag{3.1}$$

where C_s, is the capacitance of semiconductor, ε_o is the vacuum permittivity, and μ_{SAMs} is the SAM dipole moment. The thickness t_s of the QD layer is about 30 nm and the diameter of PbS QDs is around 3.6 nm which corresponds to a molecular area A of about 13 nm^2. The dielectric coefficient of PbS QDs has been reported as ε_s = 22.5, obtained from capacitance measurement.[18] In equation (3.1), the dielectric constant ε_d and the SAM thickness t_d are 2.27 and 0.45 nm, respectively. The threshold voltage shift was calculated to be -23.5 V, which is very close to the experimental result of -23.6 V for holes. The threshold voltage shift for electrons according to our experiment is -14.1 V, which shows a little deviation with respect to the result of the calculation. This deviation may originate either from the approximated model used in the equation (3.1) or the magnitude of semiconductor capacitance C_s, which is influenced by traps thus overestimating the calculated value. These results explain in addition by the improvement of the QD assembly organization, the use of HMDS SAMs is able to reduce the threshold voltage for electron accumulation.

3.3 Cytop Gating in PbS QD-FETs

After having studied the devices using bottom gate structure, the FETs using Cytop as top gate dielectric were operated (Figure 3.1). Cytop is a perfluoropolymer with chemical structure displayed in Figure 3.8 (a). The water contact angle of 115° demonstrated in Figure 3.8 (b) reveals that Cytop has hydrophobic properties.

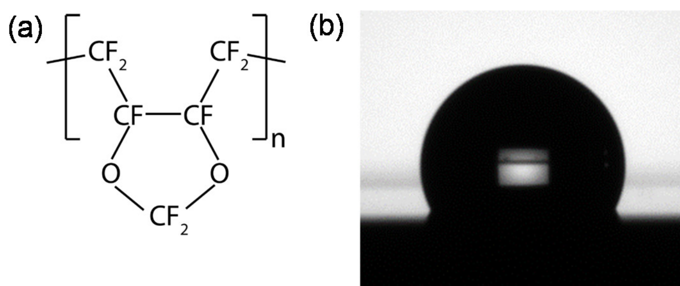

Figure 3.8 (a) Chemical structure and (b) water contact angle of Cytop.

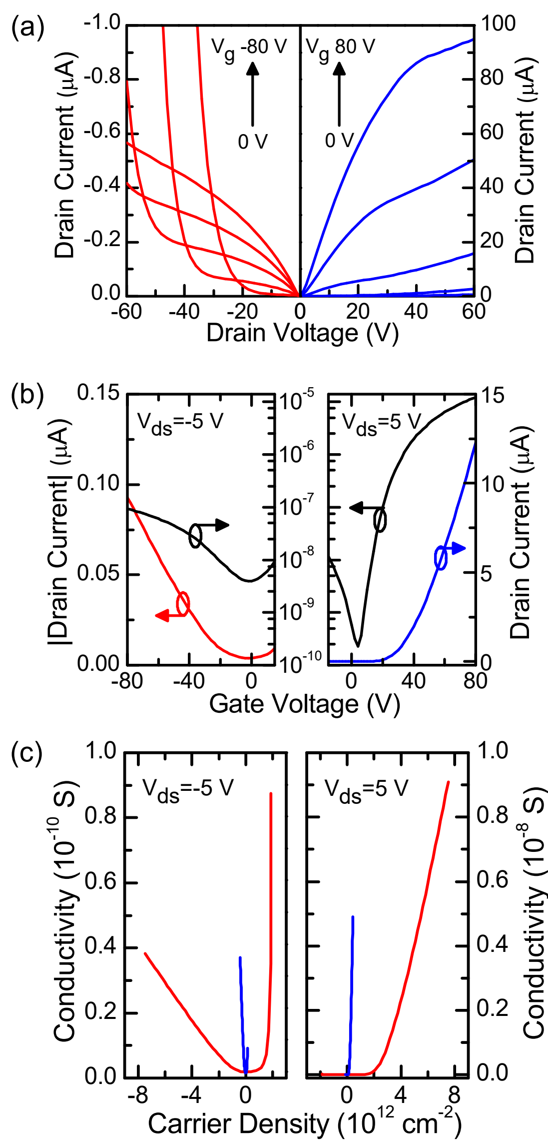

Figure 3.9 (a) I_{ds}-V_{ds} output and (b) I_{ds}-V_g transfer characteristics of PbS QD-FETs employing Cytop gate dielectric. (c) Comparison of conductivity versus carrier density in the devices with HMDS-treated SiO_2 (red) and Cytop (blue).

Figure 3.9 (a) and (b) show the I_{ds}-V_{ds} and I_{ds}-V_g characteristics of the FETs with Cytop gating. The transistors display ambipolar characteristics dominated by electron transport. In general, the I-V characteristics look very similar to the one measured by operating the devices with SiO_2 gate dielectric. This indicates that the deposition of the fluoropolymer does not introduce any unwanted chemical

reaction with the active layer. The devices show electron on/off ratio up to 10^5 and a subthreshold swing of 6.4 V·dec^{-1}. The threshold voltages for electron and hole accumulations are rather high, 37.2 V and -20.7 V, respectively. However, it is important to mention that the Cytop gate dielectric is overwhelmingly thick (2 μm) and makes the capacitance rather small (0.86 nF/cm^2). As a result, the field-induced sheet carrier density was only $n = 4\times10^{11}$ cm^{-2} at $V_g = 80$ V. This value is much smaller than the carrier density that could be induced with the SiO_2 gating ($n = 8\times10^{12}$ cm^{-2} at $V_g = 80$ V). This is the reason behind the smaller on/off ratio and the higher threshold voltage in the Cytop gate operation.

Figure 3.9 (c) compares conductivity versus carrier density induced with Cytop and HMDS-treated SiO_2. This plot shows that the threshold carrier density for electron accumulation using Cytop gate dielectric is much smaller than the accumulation using HMDS-treated SiO_2. The electron and hole mobility in the linear regime of the transistor operation is as high as 0.2 cm^{2}V^{-1}s^{-1} and 8×10^{-4} cm^{2}V^{-1}s^{-1}, respectively. Importantly, this high mobility is achieved in PbS QD layers that still maintain the original band gap of the particles as confirmed in Figure 3.5 and therefore the transistors have an on/off ratio higher than 10^5.

3.4 Distribution of Trap DOS in PbS QD-FETs

The significant mobility improvement is attributed to the lower density of trap states at the PbS/Cytop interface. Despite the lower induced carrier density, the Cytop gated FETs can maintain a conductivity as high as the SiO_2-gated and HMDS-treated SiO_2-gated FETs as shown in Figure 3.9 (c). Figure 3.10 shows the analyzed trap density of states (trap DOS) for the ambipolar transistors shown in Figure 3.4 (b), Figure 3.6 (a) (with HMDS-treated and bare SiO_2 gate) and Figure 3.9 (b) (with Cytop gating). The analysis uses a numerical model developed by Oberhoff et al., which solves the coupled drift diffusion equations governing the charge transport in semiconductors, incorporating an arbitrary distribution of trap states in the band gap.[19] The analysis has been done for the n- as well as the p-type transport. The range of validity of the trap DOS analysis (solid lines) has been estimated from the position of the Fermi level at the lowest and highest measured source-drain current. Therefore, the range of validity is narrower on the HOMO (highest occupied molecular orbital) side, where the p-type charge transport occurs. After treatment of the bare SiO_2 surface with HMDS there is a clear reduction of the trap DOS close to the LUMO (lowest unoccupied molecular orbital), whereas on the HOMO side there is no reduction of the trap DOS visible, a slight increase has even been calculated. This is in line with the measurement of the mobility: for the n-type transport the mobility increases by more than a factor of 3 (0.02 cm^{2}V^{-1}s^{-1} → 0.07 cm^{2}V^{-1}s^{-1}), whereas for the p-type transport the mobility is constant at 5×10^{-5} cm^{2}V^{-1}s^{-1}. This leads to a conclusion that HMDS can

reduce the trap DOS on the LUMO side only by passivating the SiO_2 surface. The calculated trap DOS for the bottom gate structures is comparable to results obtained for polycrystalline organic thin-films.[20–22]

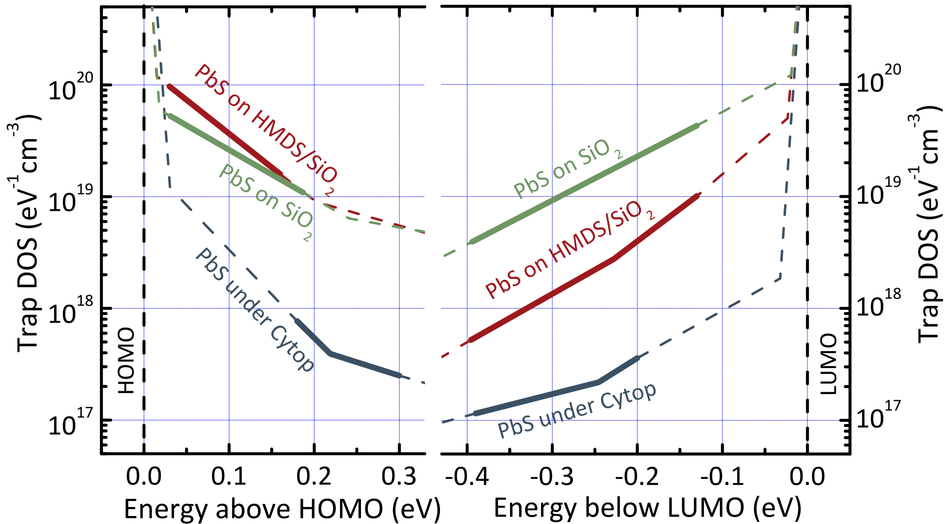

Figure 3.10 Comparison of trap DOS in PbS QD-FETs with SiO_2, HMDS/SiO_2, and Cytop gate dielectrics. The use of Cytop leads to a drastically reduced density of trap states close to both transport levels.

When the top gate configuration with Cytop gate dielectric was operated, a drastic reduction of the trap DOS over the whole measured energy range by more than one order of magnitude for both HOMO and LUMO sides was observed. This is in line with the improvement of the p-type as well as n-type mobility by one order of magnitude in this configuration. The Cytop top gate structure reduces the density of trap states clearly below the level of organic polycrystalline thin-films, therefore the trap density is closer to pentacene single crystals.[23] Quantitatively, by integrating the trap DOS over the energy, the trap density of electrons and holes in PbS QD ambipolar FETs with Cytop gating are 2.49×10^{17} cm^{-3} and 1.20×10^{18} cm^{-3}, respectively. The values correspond to 3.96×10^{11} cm^{-2} and 1.13×10^{12} cm^{-2} sheet trap densities for electrons and holes, respectively. These values are comparable to the free carrier density for electrons about 4×10^{11} cm^{-2}. These results demonstrate a high potential of solution processed PbS QDs when they are combined with appropriate materials, which reduce the density of trap states.

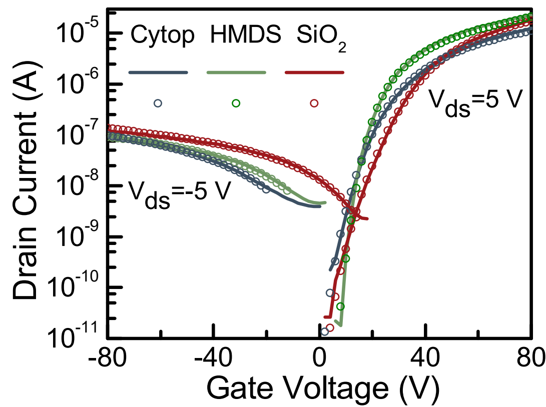

Figure 3.11 The measured and simulated transfer curves for all investigated FETs.

The reliability of the calculated trap DOS results is shown by a good fitting of the simulated transfer characteristics to the measured ones as displayed in Figure 3.11. In addition, these results are compared with the trap DOS extraction done using transient photovoltage and thermal admittance spectroscopy (TAS) measurements on quantum dot solar cell structures.[24,25] The measurements done on solar cells are sensitive to the trap DOS in the bulk of the semiconductor whereas the FETs probe the trap DOS at the interface to the dielectric as well as in the bulk. Energy wise, transient photovoltage measurements can only measure trap states in the middle of the band gap, whereas the data from FETs cover an energy range which is closer to the respective transport level. This means, the reported trap DOS values for 3MPA-crosslinked PbS QDs cover the middle of the band gap. On the other hand, the TAS measured trap DOS values for EDT-crosslinked PbS QDs cover the trap states close to the LUMO level only.[24] In contrast, these results show the complete picture of the trap DOS for both transport levels. The comparison of the top gate configuration (Cytop) with the reported bulk measurements reveals the trap DOS at 0.3-0.4 eV away from the LUMO to be in the same order of magnitude. This leads to the conclusion that the use of Cytop results in a trap DOS which is limited by the number of trap states in the bulk only and therefore the number of trap states at the interface to the Cytop dielectric is rather low. Thus, this very low density of trap states in the top gate configuration using Cytop is the microscopic origin of the improved mobility for n- as well as p-type charge carriers. Further reduction of the number of carrier traps will allow the achievement of the mobility values close to the case where almost all carrier traps are completely filled.[4]

3.5 Conclusion

Ambipolar PbS QD-FETs with improved particle assembly organization were fabricated. Through the utilization of HMDS SAMs, the interface trap density was reduced and better QD arrays on the SiO_2 surface were achieved which led to the high on/off ratio for PbS QD-FETs. The use of hydroxyl-free Cytop as gate dielectric allowed obtaining high electron mobility up to 0.2 $cm^2V^{-1}s^{-1}$ in ambipolar FETs of PbS QDs. The high carrier mobility is attributed to a very low density of trap states at the interface, which is almost 2 orders of magnitude lower than that with conventional oxide dielectrics. The high carrier mobility and the high on/off ratio results show that the controlled assembly of PbS QDs as well as the trap density reduction is crucial for the utilization of this material system for diverse optoelectronic applications.

3.6 Methods

HMDS SAM treatment on SiO_2 substrate. 230 nm SiO_2/Si with pre-patterned interdigitated Au electrodes were used as substrates. The channel length and width of the devices were 20 μm and 10 mm, respectively. HMDS was spin-coated on the substrates, the samples were then cleaned in acetone and isopropanol before they were dried at 120°C for 10 min. Contact angles were measured to investigate the coverage of the SAMs and the hydrophobicity of the substrates. The morphology of the substrates and SAMs was measured using atomic force microscopy (Seiko Instrument Inc.) in tapping mode.

TEM and HRTEM measurement. TEM and HRTEM images were obtained using a JEOL 2011 FasTEM microscope operating at an accelerated voltage of 200 kV. The QDs were deposited on the carbon side of a holey carbon-copper TEM grid by drop-casting from a 2 mg/ml toluene solution.

Device fabrication. On the substrates that were modified by HMDS SAMs, the PbS QD films were deposited and cross-linked with 3-mercaptopropionic acid (3MPA) via a layer-by-layer (LbL) sequential spin coating technique, following previously reported procedures.[4,5] The Cytop thin film has hydrophobic properties as shown by its water contact angle of 115° in Figure 3.8 (b). Cytop is utilized as top gate dielectric, since the QD films are difficult to be deposited on very hydrophobic surfaces. Cytop (CT-809M) was spin-coated onto the fabricated PbS QD devices. The samples were then annealed at 100°C for 1 h. Finally, 30 nm Al was evaporated to fabricate the top gate electrode. All device fabrication processes were performed in an N_2-filled glove box.

Device measurements and trap DOS analysis. The transistor electrical characterizations were performed using an electrical probe station

(placed in an N_2-filled glove box) that was connected to an Agilent B1500A semiconductor parameter analyzer. To analyze the density of trap states (trap DOS), we used a numerical simulation software which was developed to calculate the trap DOS from the measured transfer curves.[19] The software is based on the mobility edge model, which assumes the existence of a specific energy level (mobility edge) separating the mobile from trapped states. This model has been used to analyze a wide range of organic semiconductors.[20–22] Comparison of various trap DOS extraction methods demonstrated that the numerical simulation used here gives the most accurate results.[20,22]

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