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Towards Energy Efficient Memristor-based TCAM for Match-Action Processing

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***Abstract*—Match-action processors play a crucial role of communicating end-users in the Internet by computing network paths and enforcing administrator policies. The computation process uses a specialized memory called Ternary Content Addressable Memory (TCAM) to store processing rules and use header information of network packets to perform a match within a single clock cycle. Currently, TCAM memories consume huge amounts of energy resources due to the use of traditional transistor-based CMOS technology. In this article, we motivate the use of a novel component, the *memristor*, for the development of a TCAM architecture. Memristors can provide energy efficiency, non-volatility, and better resource density as compared to transistors. We have proposed a novel memristor-based TCAM architecture built upon the voltage divider principle for energy efficient match-action processing. Moreover, we have tested the performance of the memristor-based TCAM architecture using the experimental data of a novel Nb-doped $SrTiO_3$ memristor. Energy analysis of the proposed TCAM architecture for given memristor shows promising power consumption statistics of $16\ \mu W$ for a match operation and $1\ \mu W$ for a mismatch operation.**

***Index Terms*—Memristor, TCAM, Match-Action processing**

I. Introduction

The Internet is a combination of distributed network entities, i.e., hosts and end users, connecting through match-action processing units. These match-action processors, like switches and routers, implement complex network functions, like routing, on incoming network traffic before forwarding on the appropriate output links. Owing to the high data speed requirements, match-action processors rely on the most critical network memory, called Ternary Content Addressable Memory (TCAM), for performing matches against the header fields of incoming network packets, e.g., IP packets. The primary benefit of TCAM is its ability of performing match operations within a single clock cycle. However, this advantage comes at the cost of high energy consumption and is typically considered as unnecessarily wasteful on-chip space utilization due to the use of traditional transistor-based technology in TCAM. The use of transistors results in volatility, excessive data movements and large space requirement in TCAM due to the inherent atomic operations of transistors.

The research in the field of solid-state electronics has developed a novel component, the memristor, for enhancing and even replacing the transistor-based architectural designs. The memristor is a non-volatile electrical component which provides energy efficient response as compared to the transistors. Moreover, memristors provide a complex computational response where the current state is dependent not only on the applied input but also on the past state, unlike the transistors. This response can be used to limit the data movements between computational and storage units and save energy resources. It also helps in enhancing the resource density and reducing on-chip packing resources by programming the memristors for required computations. This article focuses on the use of programmability of memristors for TCAM architecture design.

The research community already studied the use of memristors for TCAM, however, the previous designs focused on specific memristive materials and lack generality considering the inherent drawbacks of memristors, e.g., varying resistances with usage (aging effects), degrading resistances with time (non-resilience), material and design dependent characteristics, etc. [1]–[3]. The design of memristor-based TCAM architecture poses several research questions and challenges. A first research question is, "Can a general purpose TCAM architecture be designed using memristors instead of transistors?". Moreover, the design feasibility is coupled with the performance of the TCAM architecture. Hence, the next related research question is, "How far can a generalized memristive TCAM architecture support energy efficient computations?". Finally, it is important to analyze the tradeoffs and related design challenges for memristive architectures. Hence the last research question is, "What are the tradeoffs and challenges for memristor-based TCAM architectures?".

Our contributions include, (1) development of a generalized memristor-based TCAM architecture, (2) energy analysis of the memristor-based TCAM on experimental data of Nb-doped $SrTiO_3$ memristor, (3) understanding of the performance and tradeoffs of memristor-based TCAM.

The rest of the paper is organized as follows, Sec-II presents the background and related work. Sec-III presents the proposed system architecture and working principles. Sec-IV shows the performance of our design and Sec-V concludes the paper.

II. Background And Related Work

In this section, we discuss the TCAM operating principles and architecture, and state-of-the-art research in the domain of TCAM architecture design.

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The role of TCAM is to perform match-action operations against incoming binary bit streams of 0s and 1s. Apart from storage of 0 and 1, TCAM has a don't care bit X in its memory. The role of X is to forward a match irrespective of the input query and it helps in encoding more number of match-action rules in TCAM in the same limited amount of space. TCAM performs these operations through three hardware modules, including (1) the precharge circuit, (2) the TCAM cell module, and (3) the priority encoder. The precharge circuit supplies the voltage pulses at the start of every clock cycle in order to assess the stored bits. Bits are stored in the TCAM cell module and it is the most crucial module because it performs all the match operations and consumes the majority of energy. The role of the priority encoder is to forward the most relevant match among multiple matching entries. In this research, we focus on the TCAM cell module because it performs all the match-action operations and other modules only support its operations.

Many prior researches have focused over the use of memristors for the development of energy efficient TCAM architectures. Some of the research areas in the design of memristor-based TCAM architecture include TCAM cell designing [4], managing storage operations [5], [6], performing search functions [7] and computing read and write operations efficiently [1]. The studies in these research areas showcased the effectiveness of memristors in conserving energy at the same processing rate of one clock cycle. Some earlier research focused on the development of TCAM architectures for specific applications like regular expression matching [8], [9], network intrusion detection [10], pattern matching [2] and analog data processing [3]. This research showed that memristive TCAM can be used to deploy network functions for data analysis techniques. Lastly, some researchers focused on the incorporation of emerging hardware materials like Magnetic Tunnel Junctions (MTJ) in TCAM [11], [12]. A comparison of all related research works showed that the previous TCAM architectures have been designed for specific memristors and applications. This makes it challenging to use these designs for different memristor types in real-world conditions having variations in environmental conditions and input parameters. Hence, our research focuses on the development of a general purpose memristive TCAM design which can work on any memristive material.

III. Proposed Approach

We propose the use of memristors for storage and search operations in the TCAM architecture. In this section, we describe the system architecture and working principles of our proposed memristor-based TCAM architecture.

A. System design

Our proposed design consists of four major modules namely, the memristor module, the write module, the read module and the detector module, as shown in Fig. 1. The operations of these four modules are presented below,

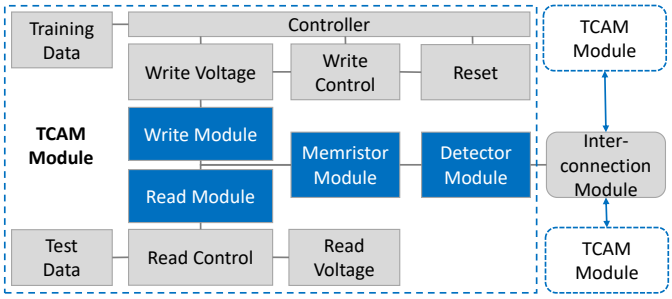

Fig. 1: The proposed memristor-based TCAM architecture.

1) Memristor module: Every TCAM cell needs to store three states including 0, 1 and X. In our research, we use two memristors to establish the complete functioning of TCAM. The memristor module consists of these two memristors coupled together for storage and search operations.

2) Write module: The function of the write module is to perform the write operations on the memristors for storing 0, 1 or X bit. Since, two memristors are used in the architecture, this module thus requires two transistors for controlling the write operations and supplying write voltages. It is pertinent to mention that our proposed architecture still relies on transistors for control operation because of three terminals in transistors which make them suitable for controllable operations.

3) Read Module: The read module is used to perform read or search operations in the proposed TCAM architecture. The role of read module is to supply read voltage pulses to the memristor module in order to estimate the stored bits in the memristor module. This module also requires two transistors in order to control the application of read voltage pulses. Our analysis showed that memristors are vulnerable to continuous voltage signals, so, separate read and write modules are required in order to ensure that the stored bits are not affected by the read operation.

4) Detector Module: The detector module plays the crucial role of acting as the voltage divider point by providing a point of operation for the whole TCAM architecture. During the operation of write module, the detector module aims to provide a path to ground in order to change the state of the memristor. During the functioning of the read module, the detector module aims to display the developed potential for providing the stored data in the memristor module.

Our proposed architecture uses these four modules through a controller module, like the traditional TCAM architecture, for managing the read and write operations by keeping a track of input data and supplying the required read and write voltages.

B. Working principles

The working operations of the proposed memristor-based TCAM architecture rely on the read and write configurations of the TCAM architecture. Fig. 2 presents the flowchart of the read and write operations in the memristor-based TCAM.

1) Write Operation: The write operation comprises of three stages. In the first stage, write control should be enabled by

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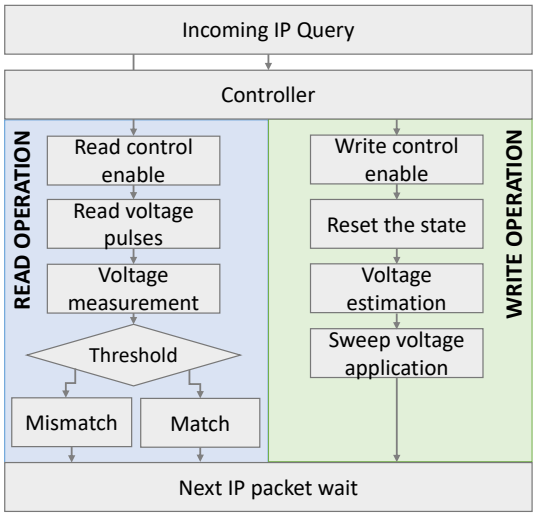

Fig. 2: Flowchart for working operations of our proposed memristor-based TCAM.

the controller in order to make sure that the system is in the write mode. In the second stage, the memristor is programmed to the initial state (reset state) in order to avoid unwanted state transitions because the next state depends on the past state and it can result in false positives during match operations. In the last stage, the required voltage based upon the requirement of 0, 1 or X bits is applied to the memristor module to complete the write operation.

2) Read Operation: The read operation also comprises of three stages in the memristor-based TCAM architecture. In the first stage, the read control is enabled by the controller. In the second stage, the read voltage pulses are applied to estimate the stored bits in the memristor. In the last stage, the voltage developed at the detector module is measured. If the measured voltage is greater than the threshold voltage, it's a match otherwise a mismatch. This match/mismatch is forwarded to the output to indicate the match-action operation.

IV. Analysis

In this section, we present the details of the memristor used for evaluations. Moreover, we present the findings on energy consumption of the proposed TCAM architecture and compare it with the state-of-the-art researches.

A. *Nb-doped $SrTiO_3$ Memristor*[1]

We have used Nb-doped $SrTiO_3$ memristors for analyzing the behavior of our proposed TCAM architecture. These memristors can exhibit multiple resistive states and it is possible to program them in different states by varying the reset and write voltages. In our initial analysis for memristor-based TCAM, we used an electrode with a cross-sectional area of 10^{-10} μm^2 inside this memristor and its I-V characteristics were analyzed in an experimental setting [13]. The result of

[1]*Nb-doped $SrTiO_3$* was developed and experimented by Anouk S. Goossens and Tamalika Banerjee, University of Groningen.

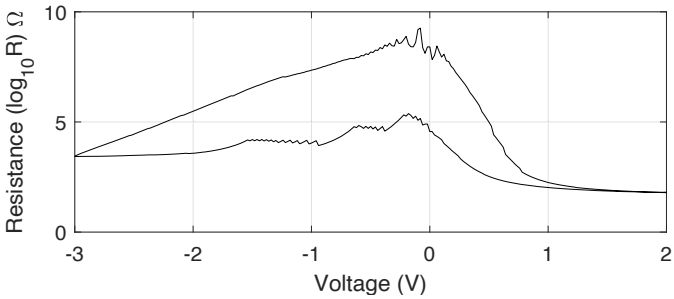

Fig. 3: Resistance patterns of Nb-doped $SrTiO_3$ memristor.

the I-V characteristics of the device in the form of resistance patterns is presented in Fig. 3. The results show that Nb-doped $SrTiO_3$ can be used to model memristive behavior in the reverse bias region due to large difference between multiple resistive states at the same voltage.

B. *Performance Analysis*

We analyzed the power consumption of our proposed memristor-based TCAM architecture using the experimental data set of Nb-doped $SrTiO_3$. The power consumption of the architecture is shown in Fig. 4. The analysis shows that the power consumption is a factor of the selected operating point (resistance) of the memristor. At any voltage level, there are two power consumption statistics which correspond to higher and lower resistance states of memristors based upon match or mismatch configuration. We perform a match using the lower resistance state and it consumes more power because a large amount of current flows through the architecture. On the other hand, the mismatch operation consumes less power because the memristor module is in a higher resistance state and very small amount of current flows through the memristor-based TCAM architecture. Overview of the analysis shows that the power consumption of the memristor-based TCAM increases upto 0.18 mW and 2.4 mW during the reverse and forward bias regions, respectively. Owing to a higher difference between lower and higher resistance states in the reverse bias region, we recommend the use of reverse bias region for selection of lower and higher resistance states.

In order to study the energy saving statistics, a subset of lower energy consumption points is presented in Fig. 5. The analysis shows that the memristor-based TCAM can provide power consumption on the order of microwatts. However, the *detection module* in our architecture is unable to function between -0.7 V and 0.7 V due to inherent operating principles of transistors. As a result, the proposed TCAM can operate at a minimum power consumption of 16 μW and 1 μW for match and mismatch operations, respectively.

C. *Comparison with state-of-the-art architectures*

The comparison of our proposed memristor-based TCAM architecture in reference to the state-of-the-art designs is shown in Table I. The results show that our proposed design can operate on a range of voltages between 0.7 V and 3 V based upon the system requirements. Moreover, the latency

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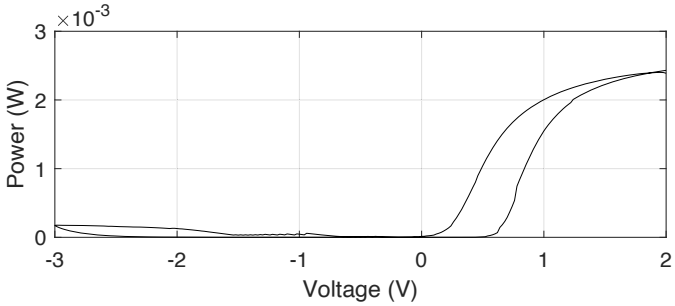

Fig. 4: Power consumption for Nb-doped $SrTiO_3$.

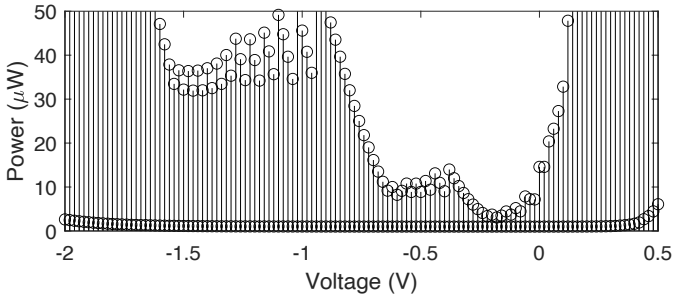

Fig. 5: Subset of power efficient points for Nb-doped $SrTiO_3$.

of our design is one clock cycle. Hence, the system running at 1 GHz provides a latency of 1 ns for our proposed architecture and our architecture supports lower clock cycles, if available. The energy consumption of our design is dependent upon the memristive material characteristics and it is equal to 1 fJ/bit and 16 fJ/bit for 1 GHz clock using Nb-doped $SrTiO_3$ memristor for mismatch and match operations, respectively. Our design is independent of the choice of memristive material, thus a change in the memristive properties, such as the resistance states, can drastically change or even reduce the energy consumption.

V. Conclusion

This work proposed the use of memristors for TCAM architecture design in order to minimize the energy consumption and space utilization inside the match-action processors. The proposed design focuses on the development of a general-purpose TCAM architecture which can suit memristive materials of all configurations. An experimental data set of Nb-doped $SrTiO_3$ memristor was used to analyze the performance of our proposed design. Preliminary findings showed promising power consumption statistics of 16 μW and 1 μW for match and mismatch operations with a latency of one clock cycle. In the future, we aim to analyze the optimal parameters and memristive configurations for the proposed memristor-based TCAM architecture.

TABLE I: Comparison of our proposed architecture with state-of-the-art designs.

Research	Config.	Voltage (V)	Latency (ns)	Energy (fJ/bit)
[14]	$16T$	0.7-1.1	1	0.58
[15]	$6T2MTJ$	1.2	0.29	1.04
[4]	$9T2M$	Upto 1.2	0.175	1.2
[16]	$16T$	1	1.9	1.98
[17]	$5T2M$	0.63-1.5	2.3	3
[18]	$11T3MTJ$	1.8	8	7.4
This Work	$5T2M$	0.7-3	1	Mismatch: 1 Match: 16

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