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Charge and spin transport in two-dimensional materials and their heterostructures

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DOI:
10.33612/diss.135800814

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Document Version
Publisher's PDF, also known as Version of record

Publication date:
2020

Link to publication in University of Groningen/UMCG research database

Citation for published version (APA):
Bettadahalli Nandishaiah, M. (2020). *Charge and spin transport in two-dimensional materials and their heterostructures*. University of Groningen. https://doi.org/10.33612/diss.135800814

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Download date: 19-09-2021

Summary

Today, we live in a hi-tech world filled with numerous electrical gadgets: be it a compact mobile phone, or a large display television set. The basic building block in most of these electronic gadgets is a field-effect transistor (FET). A FET is a three-terminal device consisting of a gate, source, and drain electrodes; herein, a semiconductor is connected between the source and the drain electrodes, and the semiconducting channel is capacitively coupled to the gate. The operation of a FET relies on the control of the current flowing through the semiconducting channel (between source and drain electrodes) by the gate electrode. No flow of current through the semiconducting channel is regarded as '0' while a constant current flow is regarded as '1', forming the basis for defining binary bits that are used to store or compute information in electrical gadgets.

For the past 30 years, Moore's law has driven the semiconductor industry in scaling the FETs, so that our electronic gadgets can become faster and smaller. According to Moore's law, the number of FETs in an integrated circuit (IC) doubles every two years. Downscaling of a FET facilitates a higher density of FETs in an IC, faster FET performance, less power of operation, and lower cost of IC fabrication. However in the past few years, we are nearing a bottleneck in the scaling of FETs, owing to the challenges like charge current leakage between the source-drain electrodes of FET (resulting in power dissipation) as a result of the shorter semiconducting channel. According to the International Technology Roadmap for Semiconductors (ITRS), in order to continue further scaling – we need new approaches like exploring new channel materials, or new devices based on alternative logic, or a combination of these both. In this thesis, both these approaches are addressed; showcasing FETs made up of two-dimensional (2D) materials, and presenting a new device concept harnessing the spin of the electrons to store/compute logic.

Basic structural and electronic properties of 2D materials, used in this thesis are introduced in chapter 2. While in chapter 3, the concepts necessary to understand the electronic and spin transport in 2D materials are discussed. In chapter 4, the protocol for fabricating FETs and heterostructures of 2D materials studied in this thesis, are presented. Additionally, the electrical and magnetic characterisation experimental setups and techniques, used to study the 2D flakes and their heterostructures, are briefly outlined in chapter 4.

From scaling theory, it is predicted that a FET with a thin oxide dielectric and a thin gate-controlled channel region would be robust against short-channel effects down to very short gate lengths. Hence, a single layer of a 2D material, which is only an atomic layer thick, seems to be very attractive in its use as channel and oxide materials to fabricate the new generation of FETs. In 2004, Andre K Geim and K S Novoselov discovered the first 2D material, graphene with naturally occurring atomically thin layers held by weak van der Waals forces, which could be cleaved into single layers by using just a scotch tape. Graphene promises excellent charge carrier mobility; but, it still lacks a bandgap which is required to achieve the turning ON and OFF of the FET.

In the quest of synthesising other 2D materials with bandgap: our collaborators from the University of Ioannina, Greece, have been successful in producing germanane; wherein, they substituted Ca with H in $CaGe_2$ crystals by topochemical de-intercalation. Following this,

world's first 2D germanane FET was fabricated and characterised at the University of Groningen, Netherlands, as presented in chapter 5.

To fabricate the germanane FET, multi-layer germanane of 60 nm thickness was cleaved and placed on a silicon dioxide substrate. Later, gold electrodes were deposited on the germanane in order to connect it with the electrical measurement circuit. Charge transport in both the electron and hole-doped regimes, i.e. ambipolar charge transport, was observed on passing charge current through the germanane FET. The charge current in the germanane FET could be turned ON (flowing) or OFF (not flowing) by controlling the electrical voltage bias applied across the gate, yielding an ON-OFF current ratio of up to 10^4 with charge carrier mobility of up to 70 $cm^2V^{-1}s^{-1}$ at room temperature. Both ambipolar charge transport and high ON-OFF current ratio have great potential for application in complementary metal oxide semiconductor (CMOS) circuits.

It was observed that, the flow of charge current underneath the gold electrodes in germanane was significantly affected due to the formation of high resistive Schottky barrier at the gold/germanane interface (formed when a semiconductor is brought in direct contact with a metal). One of the important challenges and scope for further investigation is to reduce the Schottky barrier to get the best performance out of germanane FETs.

Since germanane has a direct bandgap in its band structure, shining a red laser of 650 nm wavelength on germanane FET resulted in an enhancement of the magnitude of the charge current. Further, pulsing the red laser ON and OFF switched the charge current in the time scale of milliseconds; since the electrical measurement circuit used had a limited bandwidth, the actual time scale is expected to be faster than milliseconds (response of band electrons in similar systems such as in GaAs is typically faster than 1 ns). Our observation of optoelectronic response in germanane FET has promising implications in optoelectronic applications like photodiodes, phototransistors, etc..

An electron is a subatomic particle which contains not only the charge information but also an angular momentum called spin. The spin of an electron can either point in the in-plane or the out-of-plane direction, corresponding to '1' and '0' states respectively for logic applications. The electronics which is built using the spin aspect of an electron is called as spin electronics, abbreviated as spintronics. Spintronics offers low power operation and faster switching times, since the power required to switch the spin of an electron is comparatively low, and the switching speed is faster than the conventional charge-based electronics.

Realising gate tuneable spin transport in FET, acronymed Spin-FET, is the holy grail of spintronics. In this regard, recently there have been numerous theoretical predictions of using transition metal di-chalcogenides (TMD) in the proximity of graphene to induce anisotropic spin-orbit coupling (SOC) in graphene. The predictions suggest that the induced SOC can be changed by applying an electrical field across the gate, allowing one to control spin transport in graphene. Hence, based on the theoretically predicted long distant spin transport in isolated graphene coupled with the ability to tune the spin transport in graphene via an electric field applied across the gate, the TMD-graphene heterostructure appears to be the way forward towards realising the Spin-FET. In this direction, we fabricated and studied various TMD heterostructures such as WSe_2 and WS_2 with single and bi-layer graphene on SiO_2 substrate.

These heterostructures are contacted by the ferromagnetic cobalt electrodes whose magnetisation can be flipped by applying an external magnetic field, enabling one to inject either the in-plane or the out-of-plane electron spins into graphene.

In chapter 6, a heterostructure of multilayer WSe_2 on single-layer graphene (SLG) was studied wherein a part of graphene was covered by WSe_2. In the region of graphene covered by WSe_2, a spin lifetime anisotropy for the in-plane ($\tau_{\parallel}$) and the out-of-plane ($\tau_{\perp}$) spin transport was observed with their ratio being $\tau_{\perp}/\tau_{\parallel} = 3.5$. Also in the WSe_2 covered graphene region, we observed that the non-local resistance (R_{NL}) measured for the in-plane spin transport was tuneable by applying an electric field across the gate. However, it is not clear if the change in R_{NL} for the in-plane spin transport is due to the change in SOC or the change in spin resistance at the graphene/WSe_2 interface; and hence, it requires further investigation. Interestingly, the effect of spin lifetime anisotropy, observed in the graphene region covered by WSe_2, was also observable in the neighbouring region of graphene not covered by WSe_2 due to the diffusive nature of the itinerant spins which could explore the WSe_2 covered graphene region. When the WSe_2 coverage of graphene was longer than 3 μm, no in-plane spin transport was observed across the WSe_2 covered graphene region, alluding to a large magnitude of the SOC induced by WSe_2 in graphene. Multi-layer WSe_2 was also used as an intermediate layer for spin injection into graphene; this makes the use of TMDs as a tunnel barrier, for spin injection into graphene, interesting to study further.

In chapter 7, spin transport properties in BLG which are spin-orbit coupled to a multi-layer WS_2 with WS_2 also being used as a substrate was studied. We measured a record spin lifetime anisotropy of $\tau_{\perp}/\tau_{\parallel} \approx 40\text{-}70$ on these heterostructures. We could not tune the electric field via the back gate in BLG due to the thick WS_2 substrate; however, a workaround to use the top gate instead of the back gate needs to be explored. Furthermore, we developed a new tool called the Oblique spin-valve measurement to measure the anisotropic spin lifetime ratio by exploiting the shape-anisotropy of the ferromagnetic electrodes. The observation of high $\tau_{\perp}$ and high spin lifetime anisotropy are clear signatures of the strong spin-valley coupling for the out-of-plane spins in BLG/WS_2 systems in the presence of SOC.

In chapter 8, the spin transport properties in bi-layer graphene (BLG) which is spin-orbit coupled to a multi-layer WSe_2 was studied in a similar geometry as that of SLG/WSe_2 heterostructure. A spin lifetime anisotropic ratio of $\tau_{\perp}/\tau_{\parallel} = 3.6$ was observed in the region of BLG covered by WSe_2 and its effect was also observable in the BLG region not covered by WSe_2, but close to WSe_2 covered BLG region, similar to that observed for the SLG/WSe_2 heterostructure. Further, FETs of WSe_2/BLG in vertical geometry were also realised and studied which showed an n-type behaviour with a current ON-OFF ratio $>10^3$. The realisation of vertical FETs of graphene with TMD heterostructures unlocks their potential for developing ultra-thin electronic devices by utilising new device geometries.

Our experimental observation of strong anisotropic SOC present in both the SLG and BLG with TMD heterostructures, showing an anisotropic spin relaxation time for the in-plane and the out-of-plane spins, is one step closer towards realising next generation spintronic devices like Spin-FETs.