Charge and spin transport in two-dimensional materials and their heterostructures

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4 Experimental methods

Abstract

In this chapter, the fabrication and the characterisations performed on the nano-electronic devices are introduced. To start with, different device geometries of two-dimensional (2D) materials studied in this thesis are presented. Further, the preparation of the silicon and the Polydimethylsiloxane (PDMS) substrates are briefly explained, along with an introduction into the mechanical exfoliation of 2D flakes on these substrates. Subsequently, the process of determining the thickness of the 2D flakes using optical microscopy and atomic force microscopy (AFM) measurements is described. Later, the preparation of the 2D heterostructures using pick-up technique is described. The designing and the deposition of electrodes on 2D flakes and their heterostructures are introduced. Finally, the experimental characterisation setup and the electrical/magnetic characterisation techniques used to study the 2D flakes and their heterostructures presented in this thesis are discussed.

4.1 Sample preparation

In this section, the step-by-step fabrication of germanane transistors and graphene spin-valves studied in this thesis is discussed. The device schematic of these nano-electronic devices fabricated on 300 nm SiO_2 substrate is shown in Figure 4.1-1:

- Device (a) – multi-layered germanane contacted with Ti/Au electrodes
- Device (b) – top WSe_2/graphene heterostructure contacted with AlO_x/Co electrodes.
- Device (c) – top WSe_2/bi-layer graphene heterostructure contacted with AlO_x/Co electrodes.
- Device (d) – top hBN/bi-layer graphene/bottom-WS_2 heterostructure contacted with AlO_x/Co electrodes.

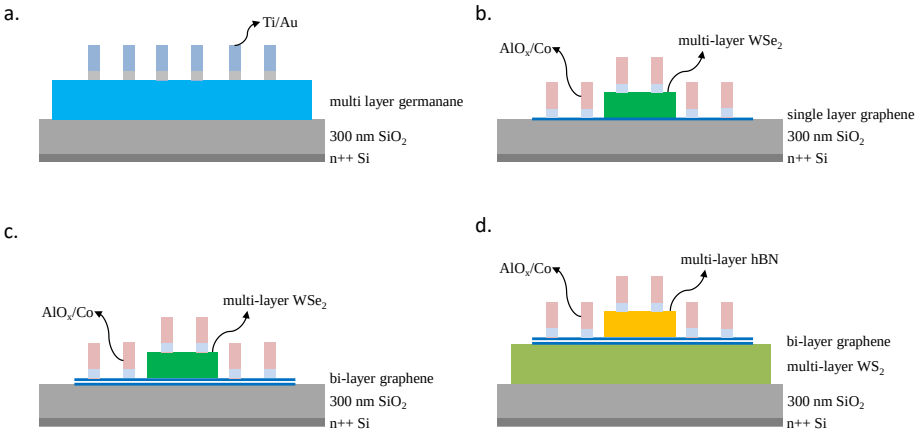

Figure 4.1-1 Device schematic of (a) Germanane transistor, (b) Graphene spin-valve, (c) and (d) bi-layer graphene spin-valve with TMD heterostructure.

4.1.1 Substrate preparation

Silicon substrate

The silicon wafer used for the device fabrication is as shown in Figure 4.1-2 and these silicon wafers are procured from Siliconquest®. The used wafer is a ~500 µm thick, highly n-doped silicon (n++ Si) with 300 nm thick SiO_2 on either sides. One of the sides is polished, and the other is etched; the polished side is used for the device fabrication. The n++ Si is used as a gate electrode with a resistivity of 0.001 Ω-cm and SiO_2 is used as an insulating layer. The capacitance offered by the n++ Si/SiO_2 substrate is ~110 µFm^{-2}. The wafer disc is 4 inches in diameter and are cut into small pieces, referred to as chips or die, of 0.8 cm (length by width) using a diamond tip scriber or a wafer cutting machine, as shown in Figure 4.1-2. The chips are then cleaned in a solution of acetone, followed by isopropyl alcohol (IPA), in an ultra-sonicate bath for 2 minutes each to remove organic residues. The cleaned chips are blow-dried with nitrogen (N_2) and annealed in a furnace at 180 ℃ for 10 minutes in order to

remove any solvent or moisture from its surface.

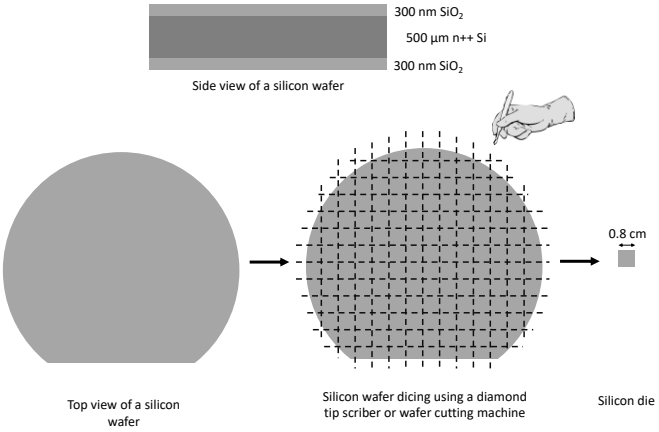

Figure 4.1-2 Illustration of a silicon wafer cut into dies/chips.

Markers, used to determine the position of the exfoliated two-dimensional flakes on the substrate during device fabrication, are deposited on the silicon chips (Ti/Au) as shown in Figure 4.1-3. These markers are designed using AUTOCAD© software and then transferred onto the substrate using a DUV (deep ultraviolet) photo-lithography tool. The markers, marked by Ti/Au (5/60 nm), are deposited on the chips by physical vapour deposition. The markers consist of numbers representing the position in x and y direction to locate the flake on the chip, and the symbol '∟' indicates the orientation of the chip.

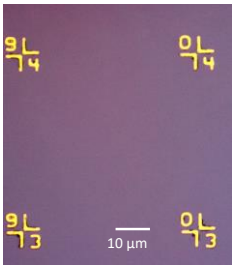

Figure 4.1-3 An optical image of a silicon chip with position (numbers) and alignment (∟) markers. The scale bar, shown with a white line is 10 µm long.

Polydimethylsiloxane substrate

Polydimethylsiloxane (PDMS) is used as a substrate for exfoliating two-dimensional materials. To prepare the PDMS substrates, PDMS monomer is mixed with a curing agent like Sylgard in 10:1 ratio, and poured into a petri dish. The petri dish is then placed in a degassing chamber to remove any bubbles in the PDMS solution. Later the petri dish with the PDMS is annealed in an oven at 60℃ for 8 hours. Finally, the PDMS is cut into appropriate size using a scalpel and is later gently peeled from the petri dish using a tweezer.

4.1.2 Mechanical exfoliation

Two dimensional (2D) materials are layered and the individual layers are held together by weak van der Waals force. By applying suitable force, one can overcome this weak interlayer force and cleave multiple layers down to a single layer. In 1999, Lu et al.[1] made efforts to thin down graphite using an atomic force microscope (AFM) tip to obtain single or multilayer graphene which they wanted to roll into carbon nanotubes. However, they were only able to obtain graphite of thickness 100 to 200 nm. In 2004, Novoselov et al.[2] used a rather naive technique of mechanically cleaving the graphite using a scotch tape, and they were successful in cleaving the graphite down to a single layer of graphene on a silicon substrate. This mechanical exfoliation technique using scotch tape can be used to cleave thin layers of any 2D material.

The 2D materials studied in this thesis are germanane, graphene, hBN, WS_2 and WSe_2. Graphene is exfoliated from highly oriented pyrolytic graphite (HOPG) crystals; WS_2 and WSe_2 appear in crystal forms and other 2D materials like germanane and hBN appear in powder forms. A tweezer or a spatula is used to handle the crystals or powders of 2D materials.

For mechanical exfoliation, a piece of scotch tape is placed on the 2D material to be exfoliated, as shown in Figure 4.1-4, and later the scotch tape is peeled. The peeled scotch tape is placed on the substrate (silicon or PDMS) and gently pressed. Finally, the scotch tape is peeled off the substrate leaving behind thin flakes of 2D material. Single-layer of 2D materials can be achieved by calibrating the choice of the scotch tape, amount of force applied, and the number of exfoliations.

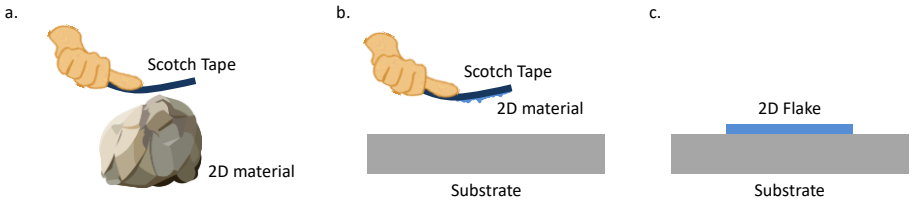

Figure 4.1-4 Multiple steps illustrating the mechanical exfoliation of a 2D flake on to a substrate (either silicon or PDMS).

Note: Exfoliation on a PDMS substrate yields relatively large area and thinner flakes compared to the exfoliation on a silicon substrate.

Mechanical exfoliation is not a reliable technique due to its uncertainty over reproducibility and inefficiency in its integration into large-area fabrication. For large-area 2D material coverage on substrates, one should consider 2D materials grown with chemical vapor deposition (CVD) technique[3].

4.1.3 Optical image

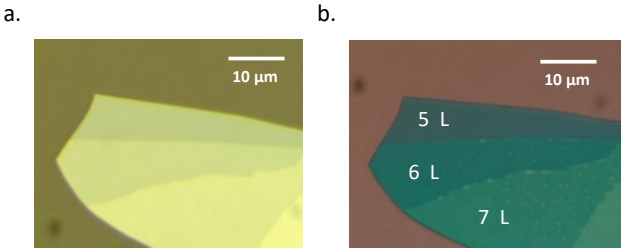

Figure 4.1-5 Optical images of a WSe_2 flake with multiple numbers of layers exfoliated on (a) PDMS, and (b) 300 nm SiO_2 substrate; L represents the number of layers, and one can see that 5 L, 6 L and 7 L have different optical contrast.

An optical image of the 2D flake is taken by placing the chip with the flakes under an optical microscope. The optical images of the 2D flakes (of WSe_2) exfoliated on a PDMS substrate and a 300 nm thick SiO_2 substrate, are shown in Figure 4.1-5. A contrast in optical reflectivity (called the optical contrast) for different thicknesses of WSe_2 on different substrates can be seen in the figure. Apart from the thickness of the flake, the optical contrast also depends on the SiO_2 thickness (in case of the silicon substrate) and the wavelength of the light source used for optical microscopy.

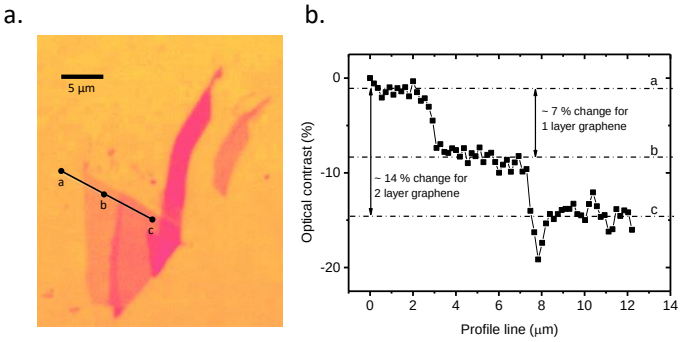

Figure 4.1-6 (a). Optical image of a few-layers graphene flake exfoliated on a 300 nm SiO_2 substrate. (b). Optical contrast for single and bi-layer graphene along the profile line a-b-c in panel (a).

The optical image and the optical contrast for graphene on a 300 nm SiO_2 substrate are shown in Figure 4.1-6. Here, we see a 7% change in the optical contrast for the single-layer graphene; while it is twice i.e. 14% for the bi-layer graphene. The 2D flake chosen for the device fabrication usually has length >10 µm and width >3 µm with desired flake thickness; further, the 2D flake is expected to be isolated without any other neighbouring 2D flakes.

4.1.4 Atomic force microscopy

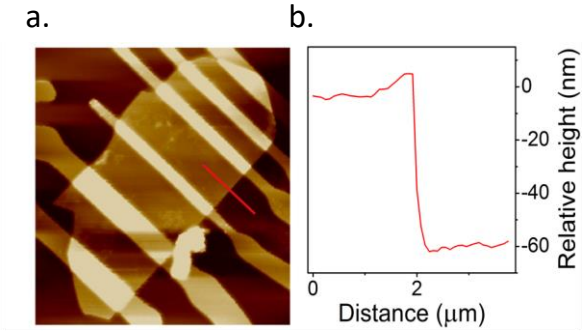

Figure 4.1-7 (a). AFM image of a germanane flake on a 300 nm SiO_2 substrate contacted with Ti/Au electrodes. (b). Height profile of the germanane flake along the red line in panel (a).

The 2D flake on a silicon substrate is profiled under an atomic force microscope (AFM) to determine its thickness. The AFM measurement of a 2D flake is done using a gold (Au) cantilever tip in contact mode. Image analysis software like Gwyddion® is used to calculate the height or thickness of the flake. Typical Gwyddion® image obtained by an AFM measurement of a 2D flake (of germanane) along with its height profile plot is shown in Figure 4.1-7. The thickness obtained for a 2D flake from AFM measurement can also be co-related with the optical contrast for the different number of 2D layers as in section 4.1.3; this helps in determining the thickness of a 2D flake using only optical microscopy even without performing an AFM (since AFM measurement takes relatively more time than determining the contrast by a microscope).

4.1.5 Pickup and transfer technique

Since 2D materials are held by van der Waals force, they can be easily stacked on top of each other to form heterostructures which could reveal unusual properties and new phenomena[4]. The heterostructures studied in this thesis are:

- Stack I – top WSe_2/graphene
- Stack II – top WSe_2/bi-layer graphene
- Stack III – top hBN/bi-layer graphene/bottom-WS_2

These heterostructures are fabricated using the dry pick-up transfer technique developed by Zomer et al.[5]. The set up used for the transfer is a modified ultraviolet (UV) lithography tool.

Using PDMS

To understand the dry pick-up transfer technique using PDMS, consider an example of the preparation of top-WSe_2/graphene heterostructure.

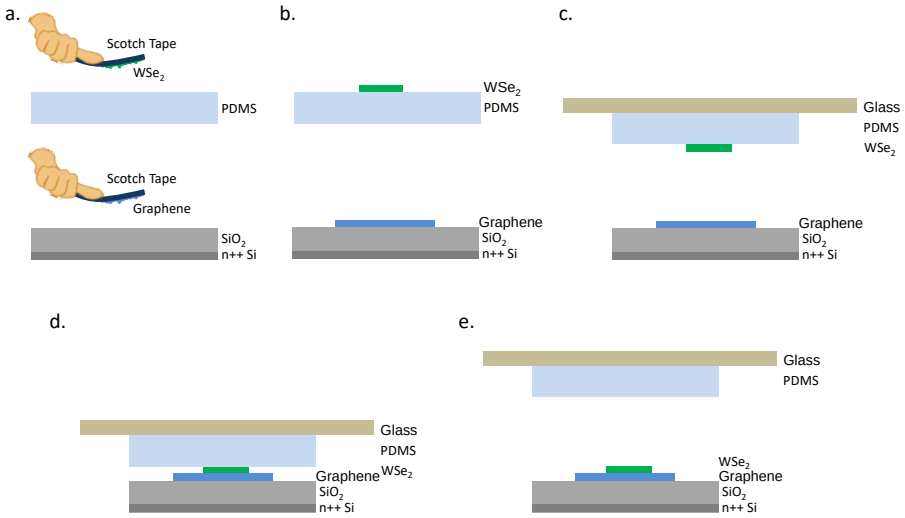

Figure 4.1-8 Step-by-step schematic of the pick-up transfer technique for realising a top-WSe_2/graphene heterostructure.

1. A WSe_2 flake is exfoliated on top of a PDMS substrate, and a graphene flake is separately exfoliated on top of a silicon substrate (300 nm SiO_2) using scotch tape as shown in Figure 4.1-8 (a) and (b).
2. The PDMS substrate is then stuck on a glass slide. In the transfer stage, this glass slide is fixed to a mask holder which is mounted under the microscope. The mask holder is an aluminium plate which can hold the glass slide by vacuum.
3. The silicon substrate exfoliated with graphene flake is stuck on an aluminium chuck situated below the mask holder. The chuck can be moved in the x-y direction using micro-manipulators.
4. The silicon substrate with graphene flake is positioned under the glass/PDMS substrate (with WSe_2 flake) using micro-manipulators as shown in Figure 4.1-8 (c). Note here that both the glass and the PDMS are transparent enabling the easy positioning.
5. The PDMS is brought in contact with the silicon substrate by moving the chuck in the z-direction (upward). The PDMS is then pressed against the silicon substrate for about 30 seconds as shown in Figure 4.1-8 (d).
6. The chuck with the silicon substrate is then lowered gently releasing it from the PDMS. The result is a heterostructure of top-WSe_2 on graphene, on top of a silicon substrate, as shown in Figure 4.1-8 (e).

Using PDMS and PC

To explain the dry pick-up transfer technique using PDMS and poly-bisphenol-A-carbonate (PC), consider an example of the preparation of top-hBN/bi-layer graphene/bottom-WS_2 heterostructure.

1. A PC solution is prepared by dissolving 6 wt.% of PC crystals in a chloroform solvent. This PC solution is drop-casted on a glass slide which is brought in contact with another glass slide to spread the PC solution across the glass slide uniformly. The glass slides are quickly separated from each other by sliding and then left in the open air to dry. This results in the formation of a thin film of PC.
2. Using scotch tape, the PC film is transferred on top of a PDMS substrate which is on a glass slide as shown in Figure 4.1-9 (a). This glass slide is fixed to a mask holder and is then mounted under the microscope in the transfer stage.

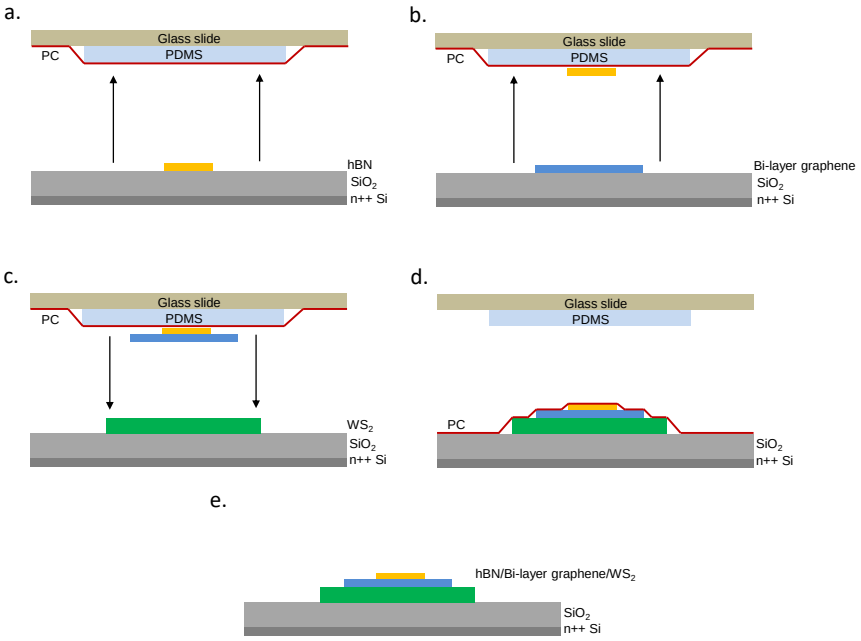

Figure 4.1-9 Step-by-step schematic of the pick-up transfer technique for realising a heterostructure of top hBN/bi-layer graphene/bottom-WS_2.

3. The hBN flake is exfoliated on top of a silicon substrate (90 nm SiO_2) using scotch tape. The silicon substrate with hBN flake is stuck on an aluminium chuck (can be moved in x-y direction) situated below the mask holder as shown in Figure 4.1-9 (a).
4. The PDMS/PC is brought in contact with the hBN flake on the silicon substrate by moving the chuck in the z-direction.
5. When the PDMS is in contact with the silicon substrate, the silicon substrate is heated to about 60-90℃ for around 30 seconds (since the chuck is equipped with a heater). Because of the heating, the PC becomes more stickier and picks up the hBN flake.
6. Next, a bi-layer graphene flake is exfoliated on top of another silicon substrate (300 nm SiO_2) using scotch tape.
7. The same process as mentioned above is used to pick up the bi-layer graphene flake

via the top-hBN as shown in Figure 4.1-9 (b). The bi-layer graphene adheres to the hBN because of the van der Waals force.

8. Later, a WS_2 flake is exfoliated on top of a new silicon substrate (300 nm SiO_2) using scotch tape.
9. Again, in order to transfer the top-hBN/bi-layer graphene on bottom-WS_2, the same process as above is followed as shown in Figure 4.1-9 (c). However, unlike heating to 60-90℃ when the PC is in contact with the WS_2 flake, the substrate is heated to 150℃ for 30 seconds. This breaks the PC from the PDMS substrate and it sticks over to the silicon substrate. Now, we have a PC covering top-hBN/bi-layer graphene/bottom-WS_2 heterostructure on top of a 300 nm SiO_2 substrate as shown in Figure 4.1-9 (d).
10. The silicon substrate with PC/heterostructure is then placed in a chloroform solution for about 6 hours. This step removes the PC by dissolving it. The silicon substrate with the heterostructure is then rinsed gently in the IPA solution to remove any PC residues.
11. Furthermore, the silicon substrate with the heterostructure is then annealed in an Ar-H_2 environment at 250-350℃ for about 3-6 hours to remove the remaining PC residues. The result is a heterostructure of top hBN/bi-layer graphene/bottom-WS_2 on a silicon substrate as shown in Figure 4.1-9 (e).

4.1.6 Electron beam lithography

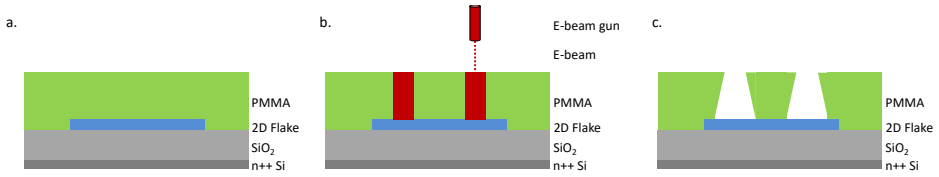

Figure 4.1-10 Illustration of the (a) Resist spin coating, (b) E-beam exposure, and (c) developing the exposed PMMA.

Electron beam lithography (EBL) uses electron beam (E-beam) to write the desired patterns over a substrate which is spin-coated with E-beam resist. In comparison to other types of lithography (extreme and deep UV lithography), EBL yields the best resolution with a feature size of ~10 nm and less. This fine resolution with E-beam is achievable due to its high incident electron energy along with its narrow beam angle which is not limited by diffraction. In this section, the EBL technique used to write patterns for the nano-electronic devices studied in this thesis is briefly described.

1. **Pre-bake** - the silicon substrate with exfoliated 2D flake is baked at 180℃ for 30 seconds on a hot plate to remove any moisture on the flake or the substrate.
2. **Resist spin coating** - Poly(methyl methacrylate) (PMMA), an E-beam resist is spun on top of the silicon substrate at 4000 RPM for 60 seconds in a spin coater. PMMA is a positive resist, i.e. the PMMA exposed by the E-beam is soluble in a solvent. The PMMA coating over the 2D flake serves a dual purpose; protecting the 2D surface against environmental degradation and also as a layer to define a pattern for electrodes. The silicon substrate with the exfoliated flake and coated by a PMMA

resist is as shown in Figure 4.1-10 (a).

3. **Post bake** – After spin coating the PMMA resist, the silicon substrate is baked at 180℃ for 30 seconds on a hot plate to dry the PMMA coating.
4. **Designing electrodes to expose** – AutoCAD® which is a computer-aided design software by Autodesk is used to draw the electrode patterns for the E-beam exposure. These drawings are then converted into a format compatible with the EBL tool.
5. **EBL exposure –** The silicon substrate with the 2D flake covered by PMMA is loaded (in a vacuum) in an EBL tool. The design of the electrodes to be exposed is loaded onto the software on a computer; this software controls the EBL tool. The design is exposed onto the PMMA using an E-beam at 10 KeV with 150 μCcm^{-2} dose as shown in the schematic of Figure 4.1-10 (b). The exposed PMMA undergoes chemical modification (polymer crosslinking) which can be removed using a suitable developer solution.
6. **Developing the exposed PMMA -** Methyl isobutyl ketone (MIBK) is mixed with IPA in 1:3 ratio to form the developer solution. The substrate with exposed PMMA is placed in the developer solution for 60 seconds and later rinsed in IPA for 30 seconds. The resulting structure of the PMMA is as shown in Figure 4.1-10 (c).

Note: Pre-bake and post bake steps are not performed in the case of fabrication of germanane transistors since germanane is temperature-sensitive.

4.1.7 Electrode deposition and lift off

Electrode deposition - Electrodes are deposited on top of the 2D flakes in a vacuum chamber (10^{-6} Torr) using electron-beam physical vapour deposition. The electrode materials deposited on different 2D flakes differ depending on what we consider to study. For example, AlO_x/Co is deposited on single or bi-layer graphene flake as shown in Figure 4.1-11 (a) to inject spins and study the spin transport in graphene. For AlO_x/Co deposition, 0.4 nm of Aluminium (Al) is deposited at a rate of 0.7 Å/s on 2D flake which is then naturally oxidized by introducing oxygen in the chamber at 10^{-1} Torr for 15 minutes to form AlO_x. This process is repeated to obtain ~0.8 nm thick AlO_x layer. Later, thick ferromagnetic cobalt (Co) of 65 nm is deposited over AlO_x. A thin Al of 3 nm is deposited as the top layer to facilitate easy electrical contact for wire bonding and prevent oxidation of Co.

In case of the germanane transistors, Titanium (5 nm) and Gold (100 nm) are deposited for studying the charge transport in germanane.

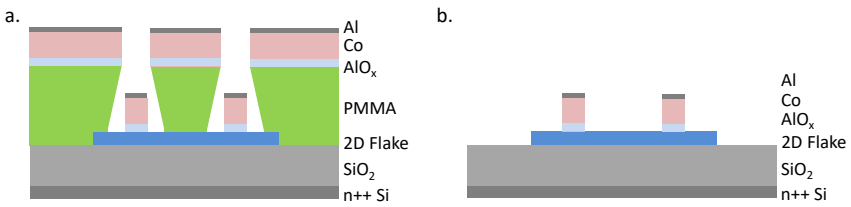

Figure 4.1-11 Schematic of the (a) electrode deposition, and (b) final device after lift-off.

Lift-off – After the deposition of the electrodes, the substrate is placed in warm acetone at 35 ℃ for 10 minutes to dissolve the resist alongside removing the overlaying excess electrode material (termed lift-off). A plastic dropper is used to agitate the unremoved or the leftover material. Later, the substrate is washed off with IPA and blow-dried with nitrogen. The chip is examined under an optical microscope to ensure the successful lift-off and to check the quality of the developed electrodes. The final device after lift-off is as shown in Figure 4.1-11 (b).

4.1.8 Wire bonding

The final device, a 2D flake or a heterostructure with electrodes on a silicon substrate, is glued on to a chip carrier using silver paste. The electrodes on the glued chip are then wire bonded to the gold pads on the chip carrier. The wire bonding is done using gold wire on a wedge-type bonding machine. The chip carrier can then be directly inserted in to an experimental characterisation setup for electrical/magnetic/optical measurements.

4.2 Electrical measurements

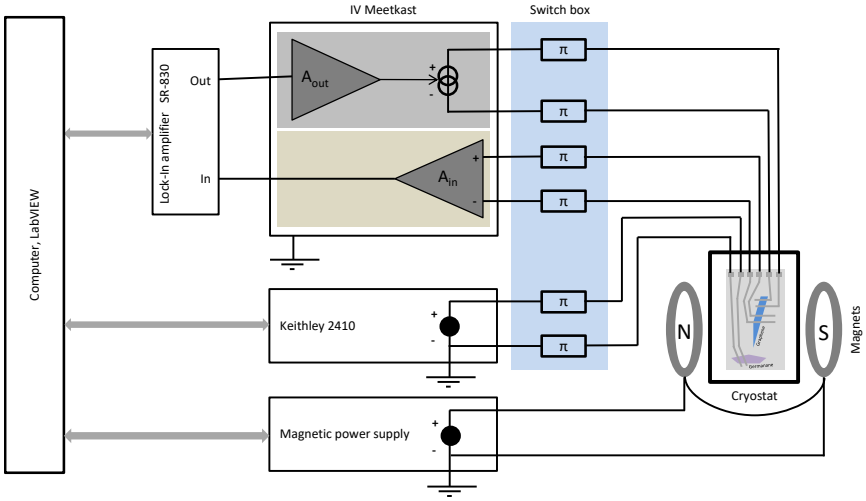

Figure 4.2-1 Schematic of the setup used to do AC and DC measurements on graphene spin-valves and germanane field-effect transistors.

For characterising the graphene spin-valves, a low-frequency lock-in detection method is used by applying an alternating current (AC) and measuring the voltage response. Whereas, for characterising germanane field-effect transistors, direct current (DC) is applied and the corresponding voltage change is recorded. A schematic of the measurement setup for both AC and DC characterisation is shown in Figure 4.2-1.

The working principle behind different parts of the setup is as explained below:

- The SR-830 is a lock-in amplifier which can generate sinusoidal voltage signal with root mean square (RMS) amplitude between 0-5 V at an oscillatory frequency range of 1 mHz – 102 kHz. A lock-in amplifier takes the input (In) signal and multiplies it with the reference signal f_{ref} (Out) and averages it over a specified time, usually in the order of milliseconds to a few seconds. The resultant signal is a DC signal, where the contribution from any signal that is not at the same frequency as the reference signal is attenuated.
- IV Meetkast is a home-made voltage-controlled current source unit. Here the IV Meetkast is controlled by the lock-in amplifier.
- Keithley 2410 is a DC voltage and current source. It can also measure the current and the voltage.
- The switch box is home-made and it connects the IV Meetkast and the Keithley 2410 to the nano-electronic device through a π filter. The π filter is a low-pass filter made up of resistor of 1 KΩ and capacitor of 10 nF; its role is to cut off high-frequency signal (i.e. it passes signal below 16 kHz). The switch box also has other modes where the sample can be connected to either float or common ground.
- Both the lock-in amplifier and the Keithley 2410 are interfaced with a computer by GPIB connectors and are controlled by the LabVIEW programme on the computer. The LabVIEW is also used to record measurements by gathering and analysing the data from the lock-in amplifier and the Keithley 2410.
- A chip carrier with the nano-electronic device is loaded on to a sample holder which is wired with the switch box. The sample holder is then placed in a cylindrical chamber which can be vacuumed. This chamber is equipped with a liquid helium flow cryostat and the chamber is fixed in between the poles of an electromagnet. The closed-cycle cryostat uses the liquid helium as the cryogenic fluid to reach temperatures as low as 4.2 K. The chamber also has a glass window through which light can be shined on the sample.
- The electromagnet from GMW systems is mounted on a rotating table; it can generate up to 1.2 T magnetic field. The power supply to the magnet is from a Sorensen DLM40-75E which can output up to 40 V and 75 A. The power supply is controlled by the LabVIEW which in-turn controls the magnetic field applied to the sample.

Operation of the setup starts by loading the sample (graphene spin-valve or the germanane transistor) on to the sample holder and then placing it in the chamber which is then vacuumed to 10^{-6} mbar. The glass window is closed with a silver foil to avoid the exposure to light.

1. **Performing a non-local SV measurement on the graphene spin-valve:** The lock-in amplifier is set to output 1 V at f_{ref} (usually at 21 Hz); this signal is fed to IV Meetkast (operating in AC in/out) where the current source is set to 1 μA range which outputs 1 μA AC. The switch box is connected to pass the current coming from the IV Meetkast to the graphene spin-valve. The measured non-local voltage is passed through the switch box and is fed to the amplifier in the IV Meetkast, which is usually set to amplify the voltage by a factor of 10^2. This amplified voltage is then available at the input of the lock-in. The wait time of the lock-in is usually set to 3 times the $1/ f_{ref}$. The voltage at f_{ref} is recorded by the LabVIEW on the computer. The voltage can also be measured as a function of the magnetic field or

the temperature which could be set in the LabVIEW software.

2. **Performing IV sweep on germanane transistor:** Keithley 2410 is programmed by the LabVIEW software to operate as a voltage source applying voltage on the sample through the switch box. The applied voltage is usually swept from +5 V to -5 V at a rate of 0.2 V/s. The measured current from the germanane transistor is then read by the Keithley 2410 which also acts as an ammeter. The applied voltage and the measured current from the Keithley 2410 are recorded by the LabVIEW on the computer. The voltage can also be measured as a function of the magnetic field or the temperature which could be set in the LabVIEW software.

4.2.1 Charge and spin transport

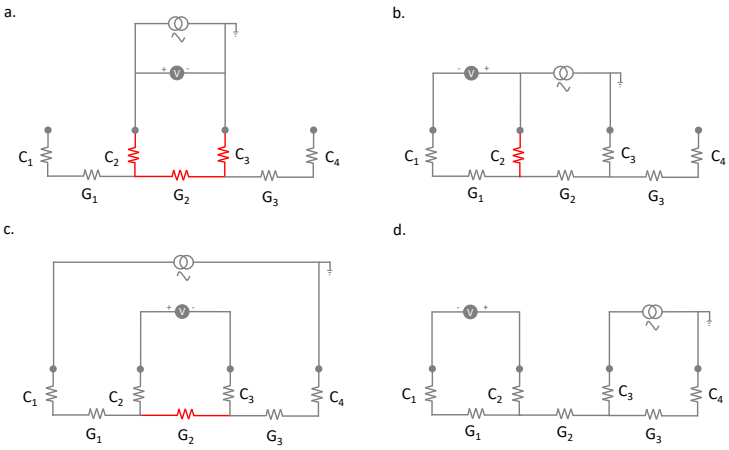

Figure 4.2-2 Resistor model for a graphene flake contacted with electrodes $C_{1,2,3,4}$ to study a. 2 terminal, b. 3 terminal, c. 4 terminal local and d. 4 terminal non-local measurements.

To understand the charge and the spin transport in 2D materials, consider a 2D flake (e.g. graphene) contacted by four electrodes as shown in Figure 4.2-2. Here, $C_{1,2,3,4}$ represents the contact resistance which includes the sum of the resistances: of the wire connected to the electrodes, of the filter in the filter box, of the electrode and of the electrode/graphene interface. $G_{1,2,3}$ represents the resistance of the graphene flake.

- 2 terminal measurement – current is passed between the pins connected to C_2 and C_3; as a result, the current flows through C_2, G_2, and C_3 as shown in Figure 4.2-2 (a). The voltage is measured across the same pins, resulting in a total measured resistance of C_2+ G_2+C_3.
- 3 terminal measurement – current is passed between the pins connected to C_2 and C_3; as a result, the current flows through C_2, G_2, and C_3 as shown in Figure 4.2-2 (b). The voltage is measured across the pins connected to C_1 and C_2, resulting in a total measured resistance of C_2.
- 4 terminal local measurement – current is passed between the pins connected to C_1

and C_4; as a result, the current flows through C_1, G_1, G_2, G_3, and C_4 as shown in Figure 4.2-2 (c). The voltage is measured across the pins connected to C_2 and C_3, resulting in a total measured resistance of G_2.

- 4 terminal non-local measurement – current is passed between the pins connected to C_3 and C_4; as a result, the current flows through C_3, G_3, and C_4 as shown in Figure 4.2-2 (d). With the use of the ferromagnetic electrodes, spin accumulation is created in the graphene at the electrode/graphene interface i.e. at C_3/G_3 and at C_4/G_3. The spin accumulation diffuses along the length of the graphene creating a difference in chemical potential underneath C_2 and C_1 which is reflected as a voltage difference measured across C_2 and C_1. Here, there is no charge current flow in the voltage detection circuit and hence the observed voltage drop is purely spin-related. Details of the non-local SV measurement and the Hanle spin precession measurement are explained in chapter 3.

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