High Mobility and Low Density of Trap States in Dual-Solid-Gated PbS Nanocrystal Field-Effect Transistors

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Semiconducting colloidal nanocrystals (CNCs) are of remarkable research interest due to their prospects for a wide range of optoelectronic devices, including solar cells,[1–3] photodetectors,[4–6] photoelectrochemical hydrogen production,[7] and light-emitting devices.[8,9] The quantum confinement of carrier wavefunctions in the NCs leads to the formation of discrete electronic energy levels and a tunability of their electronic band gaps by NC size.[10] Among a broad variety of NCs, lead sulfide (PbS) is one of the most interesting because of a well-developed stoichiometric variations obtained during or post synthesis.[18] The fabrication of field-effect transistors (FETs) is one of the best methods to evaluate charge carrier transport properties in semiconductors, including CNC assemblies.[23,24] Since FETs are interface-based devices, charge trapping is not only influenced by the properties of the active layer (the NCs assembly in this case) but also by the nature of the gate dielectric and its surface. Many efforts have been made to enhance the charge carrier mobility in PbS NC transistors. These attempts include variation of cross-linked ligands,[14–16,19] chemical post-deposition treatments to vary doping levels or to fill carrier traps,[1,18,22] increasing of the chemical purity,[10] and controlling the effect of oxygen/moisture during fabrication.[15,16] Nevertheless, the typical mobility values are still only up to 10−2 cm2 V−1 s−1, with the exception of sintered PbS NCs, which however often give rise to unipolar devices with limited on/off ratio,[18,23] and the devices which utilize ionic-liquid gating that allow to accumulate a higher carrier density than trap density.[15,26,27] In devices using conventional oxide dielectrics such as SiO2, the transport characteristics are still trap dominated.[15,16]

In this communication, we demonstrate high electron mobility and a very low trap density in ambipolar PbS NC-FETs through the improvement of the NC assembly and the utilization of an amorphous fluoropolymer (Cytop) thin film as gate dielectric. Cytop is a hydroxyl-free and transparent polymer dielectric which has a dielectric constant of 2–2.3. We first improve the assembly organization of the 3-mercaptopropionic acid (3MPA) cross-linked PbS nanocrystals on the SiO2 surface through the utilization of hexamethyldisilazane self-assembled monolayers (HMDS-SAMs). This SAM treatment passivates the silanol on the SiO2 surface that may act as electron trapping site. Cytop was deposited on top of the PbS nanocrystal assembly as second gate structure. The dual-gated FET structures using Cytop as a top gate and SiO2 as bottom gate dielectric (Figure 1a), are utilized to compare the influence of the two different dielectrics on the same PbS nanocrystal assembly. Finally, from the obtained transport characteristics, and the simulation and numerical fitting to quantify the trap density of states (trap DOS), we observe for both holes and electrons in the FETs a sheet trap density lower than 1012 cm−2, which explains the very high electron mobility of 0.2 cm2 V−1 s−1.
Deposition of PbS nanocrystal films for FETs as well as for solar cell devices, is commonly performed using a layer-by-layer method to ensure effective ligand exchange. Therefore, the assembly organization of the first nanocrystal monolayer is the most crucial factor that determines the morphology of the successive layers. We found that the conventional method for the deposition of NCs on a cleaned SiO₂, which has been used to successfully demonstrate well-performing devices, produces clusters instead of large scale homogeneous films. The clustering is observed from the first monolayer after the ligand exchange of oleic acid with 3MPA (Figure 1b). The formed clusters can be as thick as the equivalent of 3 monolayers, resulting in a root mean square (RMS) roughness of about 2.4 nm.

To increase the hydrophobicity of the substrate, we functionalized the SiO₂ surface using hexamethyldisilazane-self-assembled monolayers (HMDS-SAMs). The HMDS-functionalized SiO₂ shows a water contact angle of 60°, which is increased significantly in respect to the contact angle measured for pristine SiO₂ (30°) (S1, Supporting Information) From the AFM micrographs, the surface of HMDS-treated SiO₂ is comparably smooth as the pristine SiO₂ (S2, Supporting Information). The smoothness of the surface and the high contact angle clearly show that HMDS formed a well packed self-assembled monolayer and passivated the silanol groups on the SiO₂ surface. This functionalization significantly improves the assembly-order of the deposited PbS NCs. The RMS roughness equal to 0.8 nm indicates that no significant clustering is present in the first monolayer of the nanocrystal assembly after ligand exchange (Figure 1c). This indicates that the use of HMDS-SAMs homogeneously reduces the surface energy for the deposition of PbS nanocrystals from chloroform-based solutions.

The active layer of the field-effect transistors is composed of 5 NC monolayers providing a total thickness of 30 nm. In this study, we used PbS NCs with size of 3.6 nm (Figure S3, Supporting Information, for high resolution transmission electron microscopy (HRTEM) micrographs). The devices are completed by spin coating Cytop on the active layer and depositing Al as a gate electrode. The Cytop and Al electrode form the 2nd gate structure that will be used for charge carrier modulation, in addition to the SiO₂ gate. The PbS NC-FET prepared on HMDS-treated SiO₂ was first operated as a bottom-gated bottom-contacted FET with SiO₂ as gate dielectric. The Iᵥ–Vᵥ output characteristics of the FET with SiO₂ accumulation are shown in Figure 2(a). The FETs showed ambipolar properties with more n-dominated characteristics, consistent with our previous reports on PbS NC-FETs using 3MPA as ligands. Both, hole and electron enhancements, show clear current saturation behaviors. In the small drain voltage operation, it is obvious that the device exhibits nearly ohmic-like injection, both, for holes and electrons.

Figure 2(b) shows the Iᵥ–Vᵥ transfer characteristics of electron and hole modulations in the corresponding transistors.
The electron on/off ratio achieves a value as high as $10^6$. To our knowledge, this is the highest on/off ratio reported for PbS NC-FETs. We extracted the charge carrier mobility from the transfer characteristics of the FET operating in linear regime with the reference device, in which the PbS layers were deposited on top of bare SiO$_2$ (without HMDS-treatment) and where the clustering of the nanocrystals occurred. From the parameters extracted from the device characteristics of this reference sample (See Figure S4, Supporting Information), it can be deduced that the improvement of the nanocrystal organization led to an increase of the carrier mobility of about a factor of 3 for electrons. There is, however, no significant change in the hole accumulation. Two main differences can be observed from the comparison of the two types of devices. In the reference sample, the drain current in the n-channel saturation regime decreases with the increase of drain voltage, which is not observed in the case of the HMDS-treated sample (Figure S4, Supporting Information). This decrease of the current in the saturation regime can be attributed to the trapping of electrons. Moreover, from the comparison of the $I_D$-$V_C$ transfer curve between the HMDS-treated device and the reference device fabricated on bare SiO$_2$ (Figure 2c–d), we observed that the device with HMDS-treated SiO$_2$ shows a lower subthreshold swing ($S_S = 2.71$ Vdec$^{-1}$) than the reference device ($S_S = 6.77$ Vdec$^{-1}$). The lower subthreshold swing corresponds to a reduced interface trap density due to passivation of silanol after the HMDS treatment. Furthermore, by extracting the threshold voltage of the carrier accumulation of both devices, using the intercept linear extrapolation of drain current to the gate voltage axis, considering

$$I_{ds} = \frac{\mu C_{ox} W V_{ds}}{L} \left( V_g - V_{th} - \frac{V_{ds}}{2} \right)$$  \hspace{1cm} (2)$$

we obtained an average $V_{th}$ for bare SiO$_2$ of 41.3 V and 12.6 V for electrons and holes, respectively. The devices that were treated with HMDS-SAMs demonstrate an average threshold voltage of 27.2 V and −11 V for electrons and holes, respectively. This indicates that the HMDS-SAM treatment shifts the electron threshold voltage as much as −14.1 V and the hole threshold voltage as much as −23.6 V. The transistors that undergo the HMDS-treatment show electron doping, which indicate less trapped electrons and the effect of the introduction of interface dipoles. We calculated the influence of the attached HMDS molecules using Gaussian Program and found that the dipole moment at the SiO$_2$ surface changed by 0.61 D after the HMDS treatment (Figure S5, Supporting Information). It has been reported that the change of the dipole moment at the transistor interface can influence the threshold voltage values, where positive dipole moments shift the threshold voltages to more negative voltage, and vice versa.$^{[28]}$ The threshold voltage shift can be estimated using$^{[29,30]}$

$$\Delta V_{th} = \frac{(C_s + C_{sam}) \mu_{sam}}{\varepsilon_s \varepsilon_r C_s t_d A}$$  \hspace{1cm} (3)$$

where $C_s$ is the capacitance of the semiconductor, $\varepsilon_s$ is the vacuum permittivity, and $\mu_{sam}$ is the SAM dipole moment. The thickness $t_d$ of the semiconducting nanocrystal layer is about 30 nm and the diameter of the PbS nanocrystals is around 3.6 nm which corresponds to a molecular area $A$ of about 13 nm$^2$. The dielectric coefficient of PbS nanocrystals has been reported as $\varepsilon_s = 22.5$, obtained from capacitance measurement.$^{[31]}$ In Equation (3), we used a dielectric constant $\varepsilon_r$ and SAM thickness $t_d$ of 2.27 and 0.45 nm, respectively. We then obtained threshold voltage shift of −23.5 V, which is very close to our experimental result of −23.6 V for holes. The threshold voltage shift for electrons according to our experiment is −14.1 V, which shows a little deviation respect to the result of the calculation. This deviation may originate either from the approximated model used in the Equation (3) or the magnitude of semiconductor capacitance $C_s$, which is influenced by traps thus overestimating the calculated value. These results are explained
in addition by the improvement of the NC assembly organization, the use of HMDS-SAMs is able to reduce the threshold voltage for electron accumulation.

After having studied the devices using the bottom gate, we operated the FETs using the Cytop as top gate to modulate the charge carrier accumulation. Figure 3 (a–b) shows the \( I_D-V_G \) and \( I_D-V_C \) characteristics of the FET. The transistors display ambipolar characteristics dominated by electron transport. In general, the \( I-V \) characteristics look very similar to the one measured by operating the device with the SiO\(_2\) gate. This indicates that the deposition of the fluoropolymer does not introduce any unwanted chemical reaction with the active layer. The devices show electron on/off ratio up to \( 10^5 \) and a subthreshold swing of 6.4 V dec\(^{-1}\). The threshold voltages for electron and hole accumulation are rather high, 37.2 V and ~20.7 V, respectively. However, it is important to mention that the Cytop gate is overwhelmingly thick (2 \( \mu \)m) and made the capacitance rather small (0.86 nF cm\(^{-2}\)). As a result, the field-induced sheet carrier density was only \( n = 4 \times 10^{11} \) cm\(^{-2}\) at \( V_C = 80 \) V. This value is much smaller (more than one order of magnitude) than the carrier density that we could induce with the SiO\(_2\) gate (\( n = 8 \times 10^{12} \) cm\(^{-2}\) at \( V_C = 80 \) V). This is the reason behind the smaller on/off ratio and the higher threshold voltage observed during Cytop gate operation. Figure 3c compares the sheet conductance versus carrier density induced in Cytop and HMDS-treated SiO\(_2\). This plot shows that the threshold carrier density for electron accumulation using Cytop gate is much smaller than the accumulation using HMDS-treated SiO\(_2\). The electron and hole mobility calculated in the linear regime of the transistor operation is as high as 0.2 cm\(^2\) V\(^{-1}\) s\(^{-1}\) and \( 8 \times 10^{-4} \) cm\(^2\) V\(^{-1}\) s\(^{-1}\), respectively. This electron mobility is the highest reported for ambipolar PbS NC-FETs with solid state gate dielectrics using 3MPA ligands without sintering. Employing shorter inorganic ligands than 3MPA has allowed recently achieving higher carrier mobility with an on/off ratio of \( 10^5 \). Our PbS NC layers maintain the original band-gap of the particles (Figure S3, Supporting Information) and therefore the transistors have an on/off ratio higher than \( 10^5 \).

We attributed this significant mobility improvement to the lower density of trap states at the PbS/Cytop interface. Despite the lower induced carrier density, the Cytop-gated FET operation can maintain a sheet conductivity as high as the SiO\(_2\)-gated and HMDS-treated SiO\(_2\)-gated FETs. Figure 4 shows the analyzed density of trap states for the ambipolar transistors shown in Figure 2b, Figure 2d (with HMDS-treated and bare SiO\(_2\) gate) and Figure 3b (with Cytop gate). The analysis is using the numerical model developed by Oberhoff et al., which solves the coupled drift diffusion equations governing the charge transport in semiconductors, incorporating an arbitrary distribution of trap states in the band-gap. A more detailed description of the simulator is given in the supporting information. The analysis has been done for the n- as well as the p-type transport. The range of validity of the trap DOS analysis (solid lines) has been estimated from the position of the Fermi level at the lowest and highest measured source drain current. Therefore, the range of validity is narrower on the HOMO side, where p-type charge transport occurs. Since the discrete electronic states of NCs resemble more those of molecules, here HOMO and LUMO terminologies are used instead of conduction and valence band. After treatment of the bare SiO\(_2\) surface with HMDS there is a clear reduction of the trap DOS close to the LUMO, whereas on the HOMO side there is no reduction of the trap DOS visible, a slight increase has even been calculated. This is in line with the measurement of the mobility: for n-type transport the mobility increases by more than a factor of 3 (0.02 cm\(^2\) V\(^{-1}\) s\(^{-1}\) → 0.07 cm\(^2\) V\(^{-1}\) s\(^{-1}\)), whereas for p-type transport the mobility is constant at \( 5 \times 10^{-3} \) cm\(^2\) V\(^{-1}\) s\(^{-1}\). This leads to the conclusion that HMDS can reduce the trap DOS on the LUMO side only by passivating the SiO\(_2\) surface. The
obtained trap DOS for the bottom gate structures is comparable
to results obtained for polycrystalline thin-films.[33–36] When we use the top gate configuration with Cytop as gate
dielectric, we see a drastic reduction of the trap DOS over the
whole measured energy range by more than one order of mag-
nitude for both HOMO and LUMO sides. This is in line with
the improvement of the p-type as well as n-type mobility in
this configuration by one order of magnitude. The Cytop top
gate structure reduces the density of trap states clearly below
the level of organic polycrystalline thin-films, therefore the trap
density is closer to pentacene single-crystals.[37] Quantitatively,
by integrating the trap DOS over the energy, the trap density
electrons and holes in PbS NC ambipolar FET with Cytop
gate are 2.49 × 10^{17} \text{ cm}^{-3} and 1.20 \times 10^{18} \text{ cm}^{-3},
respectively. The values correspond to 3.96 \times 10^{11} \text{ cm}^{-2}
and 1.13 \times 10^{12} \text{ cm}^{-2} sheet trap densities for electrons and holes, respectively. These
values are comparable to the free carrier density for electrons
about 4 \times 10^{11} \text{ cm}^{-2}. To access the transport mechanism in
our films we performed temperature-dependent measurement
of the mobility (Figure S6, Supporting Information). Interest-
ingly the electron mobility with both gate dielectrics has a max-
imum between 300 K and 250 K decreasing at lower tempera-
ture (strong indication of hopping transport), while the hole
mobility reaches in both samples its maximum between 120 K
and 150 K. This complex behavior is probably determined by
the interplay of hopping transport and transport in narrow
mini-bands; a detailed analysis of it, is however not the pur-
pose of the current work.[38] This result demonstrates the high
potential of solution processed PbS NCs when they are com-
bined with appropriate materials, which reduce the density of
trap states.

These results are compared with the trap DOS extraction
done using transient photovoltage and thermal admittance
spectroscopy (TAS) measurements on quantum dot solar cell
structures.[39,40] The measurements done on solar cells are sen-
sitive to the trap DOS in the bulk of the semiconductor whereas
our field-effect transistors probe the trap DOS at the interface
of the dielectric as well as in the bulk. Energy wise, transient
photovoltage measurements can only measure trap states in
the middle of the band-gap, whereas data from field effect tran-
sistors cover an energy range which is closer to the respective
transport level. This means, the reported trap DOS values for
3MPA-crosslinked PbS NC cover the middle of the bandgap.[40]
On the other hand, the TAS measured trap DOS values for EDT-
crosslinked PbS NC cover the trap states close to the LUMO
level only.[39] In contrast, our results show the complete picture
of the trap DOS for both transport levels. The comparison of
the top gate configuration (Cytop) with the reported bulk meas-
urements reveals the trap DOS at 0.3–0.4 eV away from the
LUMO to be in the same order of magnitude. This leads to
the conclusion that using Cytop results in a trap DOS which is
limited by the number of trap states in the bulk only and therefore
the number of trap states at the interface to the Cytop dielectric
is rather low. Thus, this very low density of trap states in the
top gate configuration using Cytop is the microscopic origin of
the improved mobility for n- as well as p-type charge carriers.

Reduction of the number of carrier traps will allow the achieve-
ment of the mobility values close to the case where almost all
carrier traps are completely filled.[35] The use of thinner Cytop
layers as the gate insulator would be crucial to increase carrier
density and further improve the carrier mobility.

In conclusion, we have successfully demonstrated ambip-
olar PbS NC-FETs with improved nanocrystal organization.
Through the utilization of HMDS-SAMs, the interface trap
density was reduced and better NC arrays on the SiO2 surface
were achieved which led to the highest on/off ratio for PbS NC-
FETs. The use of hydroxyl-free Cytop as gate dielectric allows
us to obtain the highest electron mobility up to 0.2 cm^2 V^{-1} s^{-1}
in ambipolar FETs of PbS NCs with solid-state gate. The high
carrier mobility is attributed to a very low density of trap states
at the interface, which is almost 2 orders of magnitudes lower
than that of conventional oxide dielectrics. Our results, the
high carrier mobility and the high on/off ratio, show that the
controlled assembly of PbS NCs as well as the trap density
reduction is crucial for the utilization of this material system
for diverse optoelectronic applications.

Experimental Section

HMDS-SAM Treatment on SiO2 Substrate: We used 230 nm SiO2/Si
substrates with pre-patterned interdigitated Au electrodes. The channel
length and width of the devices were 20 µm and 10 mm, respectively.
HMDS was spin-coated on the SiO2 substrate, the samples were then
cleaned in acetone and isopropanol before they were dried at 120 °C for
10 min. Contact angles were measured to investigate the coverage of
the SAMs and the hydrophobicity of the substrates. The morphology of
the substrates and SAMs was measured using atomic force microscopy
(Seiko Instrument Inc.) in tapping mode.

TEM and HRTEM Measurement: TEM and HRTEM images were
obtained using a JEOL 2011 FastTEM microscope operating at an
accelerated voltage of 200 kV. The nanocrystals were deposited on the
carbon side of a holey carbon–cooper TEM grid by drop-casting from a
2 mg mL toluene solution.

Device Fabrication: On the substrates that were modified by HMDS-
SAMs, PbS nanocrystal films were deposited and cross-linked using 3-
mercaptopropionic acid via a layer-by-layer (LbL) sequential spin
coating technique, following previously reported procedures.[15,16]

The Cytop thin film has hydrophobic properties as shown by its
contact angle of 115° (S1, Supporting Information). We utilize it as
top gate dielectric, since NC films are difficult to be deposited on
very hydrophobic surfaces. Cytop (CT-809M) was spin-coated onto
the fabricated PbS NC devices. The samples were then annealed at
100 °C for 1 h. Finally, 30 nm Al was evaporated to fabricate the top gate
substrate with pre-patterned interdigitated Au electrodes. The channel
electrode. All device fabrication processes were performed in an N2-filled
glove box.

Device Measurements and Trap DOS Analysis: the transistor electrical
characterizations were performed using an electrical probe station
(placed in an N2-filled glove box) that is connected to an Agilent B1500A
semiconductor parameter analyzer.

To analyze the density of trap states (trap DOS), we used a numerical
simulation software which was developed to calculate the trap DOS from
measured transfer curves.[39] The software is based on the mobility edge
model, which assumes the existence of a specific energy level (mobility
edge) separating the mobile from trapped states. This model has been
used to analyze a wide range of organic semiconductors.[33,35,37,41]

Comparison of various trap DOS extraction methods demonstrated that
the numerical simulation used here gives the most accurate results.[34]

Supporting Information

Supporting Information is available from the Wiley Online Library or
from the author.
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