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Charge transport in dual-gate organic field-effect transistors

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The charge carrier distribution in dual-gate field-effect transistors is investigated as a function of semiconductor thickness. A good agreement with 2-dimensional numerically calculated transfer curves is obtained. For semiconductor thicknesses larger than the accumulation width, two spatially separated channels are formed. The cross-over from accumulation into depletion of the two channels in combination with a carrier density dependent mobility causes a shoulder in the transfer characteristics. A semiconducting monolayer has only a single channel. The charge carrier density, and consequently the mobility, are virtually constant and change monotonically with applied gate biases, leading to transfer curves without a shoulder. © *2012 American Institute of Physics*. [doi:10.1063/1.3677676]

Organic field-effect transistors are being investigated for their potential use in low-cost, low-end electronic circuits such as contactless identification transponders.[1–3] Most transistors are unipolar *p*-type, and they can only support holes. The threshold voltage typically is slightly positive yielding normally ON devices. Therefore, integrated circuits are based on zero-V_{GS}-load topology, whereby the gate of the load transistor is connected to its source. This topology suffers from an inherently small noise margin, which is a measure for the maximum allowed spurious signal that can be accepted by the gate while still giving the correct operation. The noise margin can dramatically be improved by using dual-gate transistors to set the threshold voltage.[4] The layout of a dual-gate transistor contains an additional gate dielectric and electrode.[5,6] The second gate electrode modifies the charge carrier distribution in the channel accumulated by the first gate. If the top gate is fixed and the bottom gate swept, the shift in the threshold voltage is given by:[7–10]

$$\Delta V_{th,bot} = -\frac{C_{top}}{C_{bot}}\Delta V_{top}, \tag{1}$$

where C_{top} and C_{bot} are the capacitances per unit area of the top and bottom dielectric, and V_{top} is the top gate bias. The largest reported integrated circuit is based on dual-gate transistors.[11] The increased noise margins more than justifies the additional process steps.

The charge transport in dual-gate transistors is not yet fully understood. The transfer curves often show a typical "shoulder", meaning that in depletion the transconductance does not monotonically decrease with increasing gate bias. This anomaly has been ascribed to the capacitance of the semiconductor.[9] To investigate the charge transport and the origin of the anomaly we fabricated dual-gate transistors where we deliberately varied the semiconductor layer thickness.

The current depends on the charge carrier density and the mobility. Both the top and bottom gates determine electrostatically the charge carrier density. A complication arises because for organic semiconductors the mobility itself depends on the charge carrier density. As a result, the common 1-dimensional (1D) approximations for the carrier distribution[12,13] cannot be used to describe the charge profile of the two interacting channels in a dual-gate transistor, and a 2D analysis is required. To numerically model the electrical transport in dual-gate transistors, a software package is required where a charge carrier dependent mobility, an injection model, and background doping can be implemented. We use the CURRY package, previously developed at Philips Research Laboratories.[14] We have fabricated dual-gate transistors with various semiconductor layer thicknesses. The electrical transport has been measured as a function of biases and transfer curves have been simulated numerically. We show that the shoulder presented by the transfer characteristics is due to the charge distribution in combination with a charge carrier density dependent field-effect mobility.

Dual-gate transistors were fabricated starting with heavily *n*-doped silicon wafers acting as a common bottom gate electrode. Thermally grown SiO_2 passivated with hexamethyldisilazane was used as bottom gate dielectric. Au source and drain electrodes were defined using conventional photolithography, using Ti (10 nm) or Cr (1 nm) as an adhesion layer. To minimize the influence of short-channel effects and contact resistances, channel lengths larger than 10 μm were used. As a semiconductor poly[2-methoxy-5-(2'-ethylhexyloxy)-1,4-phenylene vinylene] (MEH-PPV) was used. MEH-PPV was spin coated in an N_2 atmosphere from toluene (5 mg/ml). Self-assembled monolayer field-effect transistors (SAMFET) of chloro(11-(5''''-ethyl-2,2:5',2'':5'',2''':5''',2''''-quinquethien-5-yl)undecyl) dimethylsilane were self-assembled from a toluene solution.[15] Subsequently

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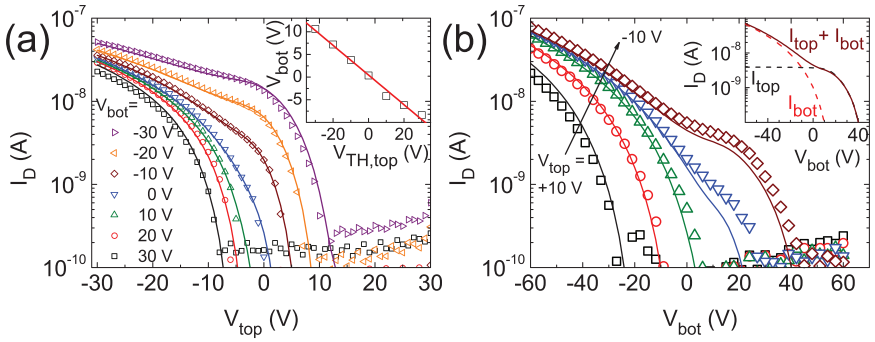

FIG. 1. (Color online) Linear transfer curves of a dual-gate transistor with a 40 nm thick semiconducting MEH-PPV layer. Measurements are presented as symbols and numerical calculations as solid lines. The drain bias was −5 V and the channel width and length were 20000 μm and 20 μm. (a) Top gate scans at fixed bottom gate biases and (b) bottom gate scans at fixed top gate biases, in V_{top} steps of 5 V. Inset in (a): top threshold voltage as a function of bottom bias. Inset in (b): calculated total current and the separate currents flowing in the top and bottom channel, for $V_{top} = -10$ V.

poly(methyl methacrylate) (PMMA) or poly(isobutyl methacrylate) (PIBMA, Sigma-Aldrich) was applied as second gate dielectric. PMMA was spin coated from butanone (50 mg/ml) and PIBMA from butanol (8% w/w). The thicknesses as measured with a Dektak 6 M Profilometer amounted to 300 nm and 600 nm respectively. The devices were finished by evaporation of a Ag or Au top gate electrode. Electrical characterization was performed in vacuum ($<10^{-4}$ mbar) and in the dark. Measurements were performed using a Keithley 4200 Semiconductor Measurement System or an Agilent 4155 C Semiconductor Parameter Analyzer.

To calculate the current in the dual-gate transistors, a mesh was defined and at each point Poisson's equation, the continuity equations and the drift-diffusion equations were iteratively solved.[14] Electrical conduction in organic semiconductors occurs by thermally activated hopping of charge carriers between localized states. The density of localized states (DOS) can be approximated by a Gaussian or an exponential energy distribution. Here, we assume an exponential DOS.[16] The local mobility then increases with carrier density, which was implemented as:[13] $\mu_p(x,y) = \mu_0 p(x,y)^{\gamma}$, where p is the hole density, γ is $T_0/T-1$, and μ_0 is a prefactor which depends on both temperature (T) and the semiconductor parameters (T_0, σ_0, and α). The boundary conditions were Ohmic contacts for holes and blocking contacts for electrons.[17,18] The relative dielectric constants used in the calculations were 3.9 for SiO_2, 2.2 for PIBMA, 3.6 for PMMA and 3 for all semiconductors (ε_{sc}).

Linear transfer curves of dual-gate transistor with a 40 nm thick MEH-PPV semiconductor are presented in Fig. 1. The top gate is swept at fixed bottom gate biases in Fig. 1(a), while in Fig. 1(b) the bottom gate is swept at fixed top gate biases. The transfer curves shift with applied fixed gate biases. The inset in Fig. 1(a) shows that the shift in threshold voltage depends on the capacitive coupling as given by Eq. (1). The shoulder in the transfer curves shown in Fig. 1(a) (Fig. 1(b)) gets more pronounced at more negative bottom (top) gate biases. For a semiconductor layer of 40 nm thick the corresponding depletion capacitance is larger than the top and bottom gate capacitances and, therefore, cannot be the origin of the shoulder.

To elucidate the origin, we numerically modeled the transport. The semiconductor thickness of 40 nm is an order of magnitude larger than the thickness of the accumulation layer, estimated to be about 2 nm.[13] Therefore, we can describe the dual-gate transistor with a spatially separated top and bottom channel. The channels have chemically dissimilar interfaces. Due to the corresponding differences in, e.g., interface roughness[6,7] and dipolar disorder,[19] the transport parameters are not identical and have to be determined separately. We take a top gate bias at the threshold voltage, here about 0 V. The source-drain current is then dominated by the bottom channel. By fitting the calculated current to the experimental data, the transport parameters for the bottom channel can be determined. A similar procedure holds for the top channel. In the simulations, we divide the film in half and assign the top and bottom transport parameters accordingly. The current is then calculated for all other combination of gate biases and presented as the solid lines in Fig. 1. A good agreement is obtained.

Parameter values extracted for the bottom channel are $T_{0,bot} = 510$ K, $\sigma_{0,bot} = 8.65\,10^6$ S/m, $\alpha^{-1} = 1.4$ Å, and for the top channel $T_{0,top} = 400$ K, $\sigma_{0,top} = 1.43\,10^5$ S/m and $\alpha^{-1} = 1.4$ Å. The parameter values are comparable to those reported previously.[13] We note that the main difference is that the mobility in the top channel is effectively a factor of five lower than that of the bottom channel. The difference can be due to differences in interface roughness and or morphology. The threshold voltages of the bottom and top channel are

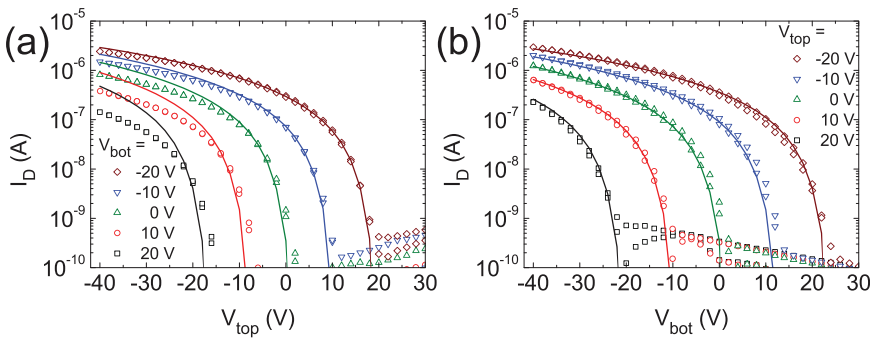

FIG. 2. (Color online) Linear transfer curves of a dual-gate SAMFET. Measurements are presented as symbols and numerical calculations as solid lines. The drain bias was −2 V and the channel width and length were 10000 μm and 10 μm. (a) Top gate scans at fixed bottom gate biases and (b) bottom gate scans at fixed top gate biases.

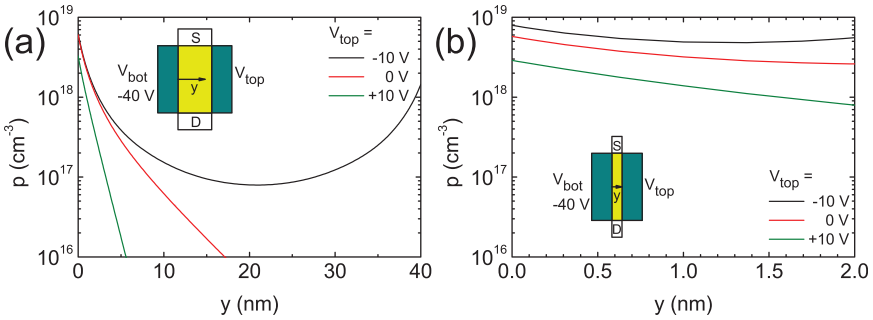

FIG. 3. (Color online) Calculated hole density in a dual-gate transistor as a function of position in the semiconductor between both gate dielectrics. The inset shows the transistor layout schematically and indicates the y-direction. A negative bottom gate bias is applied and the top gate bias is varied. The semiconductor thickness was (a) 40 nm and (b) 2 nm.

+10 V and 0 V. These values are mainly related to fixed interface charges, implemented in the numerical simulation as a layer of fixed charges at the bottom dielectric interface.

As is shown in Fig. 1, the shoulder appears at biases where one channel is in accumulation, and the other channel switches from accumulation to depletion. The origin is elucidated in the inset of Fig. 1(b). Going from negative to positive bottom bias, first the bottom channel is depleted followed by depletion of the fixed top channel. Since the average charge carrier density in the two channels is different and because the mobility is charge carrier dependent, the drain current superlinearly decreases with the increasing bottom gate bias. The carrier dependent mobility, therefore, leads to a different effective mobility in each channel, yielding a shoulder in the transfer curve.

To confirm that a shoulder is due to spatially different key transport parameters, a transistor would be required of which the layer thickness is comparable to the accumulation thickness. In that case, only a single homogeneous channel is expected. For this purpose, we fabricated a dual-gate SAMFET of which the active channel is only one monolayer thick. The transfer curves of the dual-gate SAMFET are presented in Fig. 2. The top gate is swept at fixed bottom gate biases in Fig. 2(a), while in Fig. 2(b), the bottom gate is swept at fixed top gate biases. The transfer curves shift with applied fixed gate bias in agreement with the capacitive coupling. The solid lines in Fig. 2 are now calculated using a single parameter set for the mobility function ($T_0 = 600$ K, $\sigma_0 = 1.45 \times 10^9$ S/m, $\alpha^{-1} = 1.6$ Å). A good agreement is obtained. The small deviations in accumulation (see Fig. 2(a)) might be due to a limited injection caused by under-etched electrodes.[15] For the SAMFET, the source-drain current is a monotonic function of the gate biases. No shoulder is observed while the mobility still depends on the carrier density.

The calculated charge carrier profiles, $p(y)$, for the dual-gate MEH-PPV transistor and the SAMFET are presented in Figs. 3(a) and 3(b), respectively. The bottom gate is always in accumulation. The top gate is either in accumulation (black lines), grounded (red lines) or in depletion (green lines). With both gates in accumulation, the hole density in the 40 nm thick MEH-PPV semiconductor varies over two orders of magnitude between both gates. Fig. 3(a) shows that two spatially separated channels are formed. Due to its carrier density dependence, the conductivity varies over more than two orders of magnitude. This clearly explains why the switch of one channel from depletion to accumulation gives rise to a strong increase of the current, which results in the shoulder shown in Figs. 1(a) and 1(b). For the grounded and depleted cases, the density variation is even larger. Fig. 3(b) shows that the carrier concentration in the SAMFET is confined within one order of magnitude for all biases. The charge carrier concentration in the dual-gate SAMFET is virtually constant. Only a single transport channel is formed. Hence a transition from one to two channels cannot occur and a shoulder in the transfer characteristics is absent.

In summary, the charge carrier distribution in organic dual-gate field-effect transistors has been investigated using 2D numerical simulations. A carrier density dependent mobility has been implemented. A good agreement with experimental transfer curves has been obtained. When the layer thickness is much larger than the accumulation width, two spatially separated channels are formed. The cross-over from accumulation into depletion of the two channels in combination with a different effective mobility causes a distinct shoulder in the transfer characteristics. In a dual-gate SAMFET the thickness of the semiconductor is equal to that of the accumulation layer, hence there is only one channel. The charge carrier density, and consequently the mobility, is virtually constant throughout the semiconductor and they change monotonically with applied gate biases, leading to transfer curves without a shoulder.

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