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Revealing Buried Interfaces to Understand the Origins of Threshold Voltage Shifts in Organic Field-Effect Transistors

By Simon G. J. Mathijssen, Mark-Jan Spijkman, Anne-Marije Andringa, Paul A. van Hal, Iain McCulloch, Martijn Kemerink, René A. J. Janssen, and Dago M. de Leeuw*

Charge transport in an organic field-effect transistor is dominated by the interplay between semiconductor and gate dielectric.^[1] The interactions at the interface determine the polarity^[2] and mobility^[3] of the charge carriers, control the operational stability^[4,5] and –importantly– the threshold voltage.^[1,4,6,7,8] When an organic transistor is driven with a continuous gate bias, the source-drain current is observed to decrease with time, corresponding to a shift of the threshold voltage. This shift severely limits the utilization of these devices in commercial applications. For instance, in flexible active matrix organic light-emitting diode displays a high operational stability, even exceeding that achievable with α -Si transistors,^[7] is required. On the other hand, sensors based on field-effect transistors exploit the threshold voltage shift by detecting a current change upon exposure to volatile compounds.^[9] The commonly accepted mechanism of the threshold voltage shift is charge trapping, but the actual location of these charges has remained elusive.^[10] The immobile charge can be located either in the semiconductor or in the gate dielectric. The exact location cannot easily be determined because the gate dielectric interface is buried under the semiconductor. We have now developed a very simple and effective technique to address this question in which a *p*- or *n*-type semiconductor is stripped with adhesive tape, yielding an exposed gate dielectric, accessible for various characterization techniques. Using scanning Kelvin probe microscopy^[11,12] we reveal that the trapped charges that cause the threshold shift are located at the gate dielectric and not in the semiconductor. Charging of the gate dielectric is unambiguously established by the fact that the threshold voltage shift remains, when a

pristine organic semiconductor is deposited on the exposed gate dielectric of a stressed and delaminated field-effect transistor.

Field-effect transistors were prepared on heavily doped Si wafers as common gate, covered by 200 nm thermally grown SiO₂ acting as the gate dielectric. Gold source and drain contacts were defined by conventional photolithography. The gate dielectric was passivated by a thin vapour deposited layer of hexamethyldisilazane, HMDS. As semiconductor we use poly-triarylamine (PTAA), a well-established air-stable *p*-type amorphous semiconductor that exhibits charge carrier mobilities of 10⁻³–10⁻² cm²/Vs.^[3] The chemical formula is given as inset in Figure 1a.

The active layer can be completely removed by peeling once with a piece of adhesive tape as shown by the photograph in the inset of Figure 1b. With a pair of tweezers the semiconductor can be detached as a continuous film from the gate dielectric. The reflection of the tape is visible on the bare dielectric as a bright spot. The easy exfoliation is due to the HMDS treatment, which lowers the interfacial energy; without this treatment the semiconductor cannot reliably be delaminated. The transfer curves before and after peel off are presented in Figure 1a in black and red respectively. The source-drain current after exfoliation is zero for all combinations of gate and drain biases, indicating the absence of the semiconductor.

The complete removal of the semiconductor was further verified with X-ray photoemission spectroscopy (XPS), a well-established technique to identify the chemical composition of the topmost surface layers. Nitrogen is a marker for the presence of the semiconductor, PTAA, with binding energy around 399 eV. The XPS spectra before and after delamination are presented in Figure 1b in black and red respectively. After exfoliation, no sign of nitrogen is detected on various spots on the surface. The measurements clearly demonstrate that the semiconductor can be completely removed, revealing the bare gate dielectric. Here we apply the exfoliation method to elucidate the origin of the gate bias stress effect.

First we study the gate bias stress with the semiconductor still present. In order to exclude effects from non-ideal devices, only transistors which have identical initial electrical characteristics were evaluated, here PTAA transistors. The transistors were stressed and analyzed in situ in the scanning Kelvin probe microscope (SKPM), allowing for a direct measurement of the surface potential immediately after each gate sweep. The transistors were subjected to a continuous gate bias of –60 V, source and drain electrodes were grounded. Linear transfer characteristics as a function of stress time are presented in Figure 2a together with an optical micrograph of the corresponding transistor. The transfer curves shift with stress time in the direction

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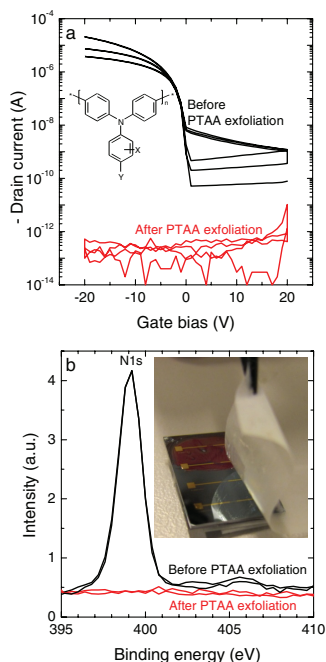


Figure 1. Exfoliation of the semiconductor. (a) Transfer characteristics before (black) and after (red) PTAA exfoliation. Drain biases were -2 V, -5 V and -20 V. The inset shows the chemical structure of polytriarylamine. X and Y are short alkyl side chains. (b) X-ray photoemission spectroscopy before (black) and after (red) PTAA exfoliation. The inset shows the actual exfoliation experiment. After exfoliation the N1s peak of nitrogen is gone, the PTAA is completely removed.

of the applied gate bias; in Figure 2a to more negative voltages. The transfer curves are nearly parallel. The main effect of gate bias stress is a shift of the threshold voltage, typical for organic transistors.^[10,13–19]

The corresponding surface potentials, measured with all electrodes grounded, are presented in Figure 2b. For the first two transfer curves, black and green, the pinch off voltage is positive. At zero volt gate bias, where the potential profile is measured, an accumulation layer is therefore present. In this case we measured a surface potential of 0 V throughout the channel. With increasing stress time, the transfer curve shifts gradually to the applied gate bias. Once the pinch off voltage shifts beyond 0 V, the surface potential becomes positive and increases with stress time.

The explanation of the evolution of the surface potential with stress time is schematically given in Figure 3. The pristine transfer curve exhibits a positive pinch off voltage, as commonly observed when using SiO_2 as gate dielectric. The origin is argued to be due to fixed negative interface charges.^[2] Upon grounding all electrodes, the interface charges are compensated by mobile holes injected into the semiconductor. The interface charges are screened and the surface potential is therefore 0 V throughout the channel, as illustrated in Figure 3a.

When a continuous gate bias is applied, the transfer curve gradually shifts to the applied gate bias, caused by trapping of charge carriers. With time, the density of positive trapped charges becomes larger than that of the negative interface charges. Consequently the pinch off voltage has shifted beyond 0 V, as in

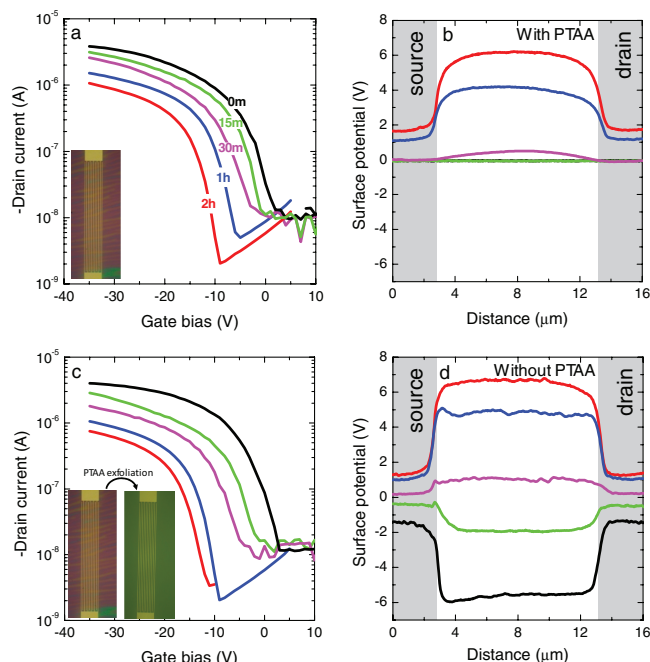


Figure 2. Charge transfer to the gate dielectric. (a) Transfer curves as a function of stress time measured at a drain bias of -5 V. The gate bias during stress was -60 V and actual times are indicated. The curves shift to the left. (b) Corresponding surface potential profiles with PTAA still present. When the pinch off voltage surpasses 0 V the surface potential becomes positive. (c) Transfer curves as a function of stress time before exfoliation. Inset: optical micrographs before (left) and after (right) exfoliation. (d) Corresponding surface potential profiles after PTAA exfoliation. The net surface potential of the negative and positive charges in the dielectric is revealed.

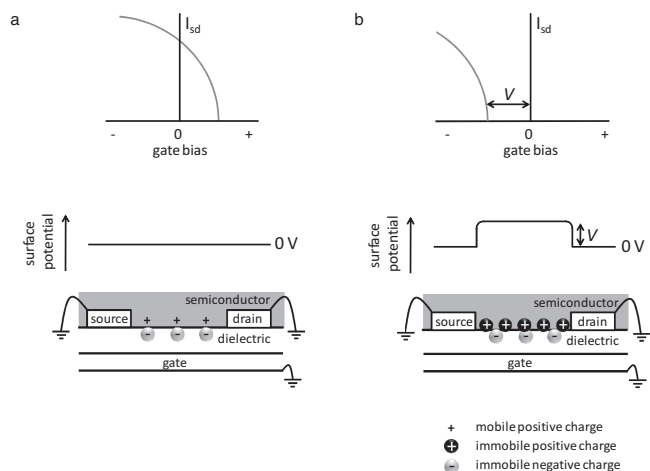


Figure 3. Schematic of the charge trapping process. (a) The top image shows a schematic representation of a transfer curve with a positive threshold voltage. A positive threshold voltage indicates that negative immobile charges are present in the gate dielectric, which are compensated by mobile holes in the semiconductor. The resulting surface potential is then zero everywhere as shown in the bottom image. (b) Schematic representation of a transfer curve with a negative threshold voltage (top), indicating that positive charges are trapped, which give rise to a positive surface potential in between source and drain as shown in the bottom image.

Figure 3b. PTAA is a *p*-type semiconductor that does not transport electrons. Therefore, when the electrodes are grounded, the immobile charges cannot be compensated. Thus, the surface potential remains non-zero and increases with the net immobile charge density and hence with the pinch off voltage. The exact molecular-level nature of these trapping sites and their location is not yet understood.^[4]

SKPM cannot distinguish between charge trapping in the dielectric or in the semiconductor.^[20] To pinpoint the exact location of the trapped charges, the semiconductor is carefully delaminated at different stages of the stress experiment. To that end, a series of PTAA transistors were stressed for specific periods. At the end a transfer curve is measured, the semiconductor is peeled off and the surface potential of the exposed gate dielectric is probed with SKPM with all electrodes grounded. The transfer curves are presented in Figure 2c with the corresponding surface potentials plotted in Figure 2d. The inset shows an optical micrograph of the transistor before and after exfoliation. The uniform change in color is caused by the complete removal of the semiconductor. We note that each transfer curve corresponds to a different device, because after peel off the transistor is destroyed. All transistors were fabricated from the same 6 inch wafer, yielding reproducible electrical characteristics.

Under applied bias the transfer curves presented in Figure 2c show a similar shift as in Figure 2a, as expected for identical devices. For the pristine transfer curve in black the pinch off voltage is positive. The surface potential measured on the bare gate dielectric is negative, in contrast to the zero potential obtained with semiconductor still present. The non-zero potential originates from the negative interface charges in the gate dielectric. There is no semiconductor to accommodate screening charges. With increasing stress time the surface potential increases. At the end of the stressing procedure the potential profiles with and without semiconductor become identical.

To determine the exact location of the trapped charges we quantitatively compare the surface potential before and after exfoliation of the semiconductor. The state of the transistor is characterized by its pinch off voltage as set by the stress time. The surface potentials as a function of pinch off voltage are presented in Figure 4a together with the corresponding schematic representation in Figure 4b. The pinch off voltage is defined as the onset of current transport. Due to a finite parasitic leakage current, the exact value cannot be determined. Therefore we arbitrarily set the pinch off voltage at the bias at which the current reaches 100 nA. The resulting offset can be disregarded for the discussion.

The pristine transistor contains negative interface charges, which are revealed upon stripping the semiconductor (region 1 in Figure 4a and Figure 4b). This demonstrates that the charges are immobile and located in the gate dielectric. When a semiconductor is present, these immobile interface charges are screened by the semiconductor leading to a zero volt surface potential (region 2 in Figure 4a and Figure 4b). For a stressed transistor a non-zero surface potential is obtained, which is the same with and without semiconductor (regions 3 and 4 in Figure 4a and Figure 4b). Upon stressing charge is trapped, which cannot be compensated by the *p*-type semiconductor.

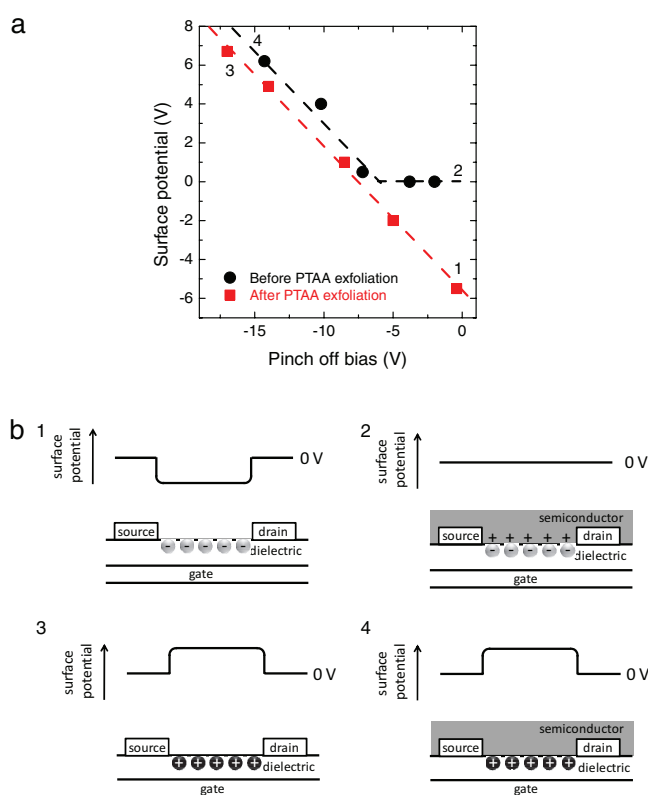


Figure 4. Quantitative comparison before and after exfoliation. (a) Surface potential extracted from Figure 2b and 2d (in the middle of the channel) versus the pinch off voltage. The pinch off voltage is defined as the bias at which the drain current reaches 100 nA. (b) Schematic representation of the position of the trapped charges with all electrodes grounded; Figure 1–4 correspond to situations labeled 1–4 in Figure 4a. For clarity only the net density of trapped charge is shown.

The surface potential is identical both with and without semiconductor, which unambiguously demonstrates for the first time that the charges are not trapped in the semiconductor but trapped in the gate dielectric.

To definitely prove that the charges are trapped in the gate dielectric, a transistor with a self-standing semiconducting film as active layer was fabricated as shown in the inset of Figure 5. The pristine transfer curve is shown in black. Subsequently the transistor is stressed until the transfer curve has shifted by about -10 V (red). The self-standing semiconducting film is then removed and a transfer curve is taken. No current is detected (green), the semiconductor is completely removed. A pristine new self-standing semiconductive film is then applied on the same source-drain electrodes. Again a transfer curve is measured and plotted in blue. The transfer curve is nearly identical to the original stressed transfer curve, proving once more that the origin of the gate bias stress effect is charge trapping in the gate dielectric.

Of course, many combinations of semiconductor and dielectric are possible. Here we focused on the most studied gate dielectric, SiO_2 , in combination with an environmentally stable amorphous polymeric semiconductor, PTAA and showed that for this system the gate bias stress effect is dominated by charge

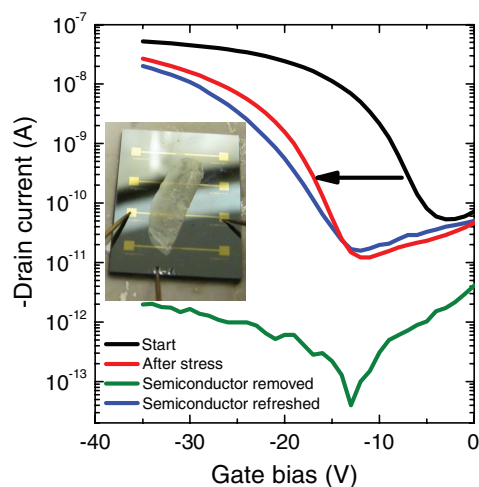


Figure 5. Refreshing the semiconductor. In black a typical transfer curve of the transistor with a self-standing semiconducting film. In red the transfer curve after the transistor is exposed to a prolonged gate bias of -60V for several minutes. In green when the semiconductor is removed. In blue a transfer curve with the self-standing semiconducting film refreshed. The invariance of the threshold voltage provides additional evidence that the charges are trapped in the gate dielectric and not in the semiconductor. Inset: photograph of the field-effect transistor with self-standing semiconducting film.

transfer into the SiO_2 gate dielectric. We have actually applied the exfoliation method to other air stable *p*- and *n*-type semiconductors, further confirming our conclusions. As an example we present a detailed study of the exfoliation experiment with perylene as semiconductor in the Supporting Information.

Gate bias stress has been studied in great detail, because it remains the primary impediment to commercial introduction of organic microelectronics. The microscopic origin has until now been under debate, possible explanations ranged from charge trapping in the semiconductor in disordered regions or at grain boundaries,^[18] charge trapping by polarization,^[21] hole-trap formation in the presence of water,^[22] to contact degradation.^[23] In these specific systems investigated, the proposed mechanisms may indeed be valid, however once they have been eliminated, the mechanism of charge trapping in the gate dielectric as described herein will pertain. This understanding will lead to development of new material sets and device architectures that can mitigate the gate bias stress effect. Some reports hint to the gate dielectric,^[15–17,24,25] however, direct experimental evidence that reveals the trapped charges in the dielectric could not be obtained.

We note that the delamination procedure can be extended to examine charge transfer across any weakly bound buried interface in a variety of device architectures. We showed that the exfoliation method can be directly transferred to other semiconductors to verify the suggested mechanisms for each particular case. The method can also be applied to other dielectrics, since the semiconductors are usually loosely bound to their gate dielectrics. Importantly, it can be applied to systems not associated with gate bias stress such as interface trapping in light-emitting diodes,^[26] photo-induced transfer across interfaces,^[17] surface dipole layers,^[1,27,28] dielectric poling,^[29,30] and sensors.^[9]

In conclusion, we have used scanning Kelvin probe microscopy on delaminated organic field-effect transistors to demonstrate that charge trapping in stressed devices does not occur in the semiconductor but in the gate dielectric, irrespective of *p*- or *n*-type operation. Charging of the gate dielectric was unambiguously established by the fact that the threshold voltage shift remained, when a pristine organic semiconductor was deposited on the exposed gate dielectric of a stressed and delaminated field-effect transistor. The exfoliation method developed for field-effect transistors can directly be utilized to study dynamic processes in variety of systems that occurs at buried interfaces that are bound by weak Van-der-Waals forces.

Experimental Section

Field-effect transistors were fabricated starting with heavily doped n^+ Si 150-mm wafers obtained from Siltronic AG. The wafers were thermally oxidized until a 200 nm oxide layer was grown. The layer thickness was confirmed by ellipsometry measurements. The substrate acts as a common gate. As source and drain electrodes a 100 nm Au layer was applied. A 10 nm Ti layer was used for adhesion. Metal electrodes were applied by sputtering using a CVC Connexion 800 sputter unit. The electrodes were defined by standard photolithography and wet etching. Subsequently the surface of the SiO_2 was exposed to a hexamethyldisilazane (HMDS) vapour for 1 hour to passivate the surface. The wafers were cut into dies of about $1 \times 2 \text{ cm}^2$. PTAA, 5%wt in toluene, was applied by spin-coating at 1000 rpm for 15s.

The electrical transport was measured using an Agilent 4155C semiconductor parameter analyzer. The electrical stressing procedure was equivalent to previous reports.^[10] The adhesive tape (Scotch, 3M) was applied over the transistor. The film was then completely removed mechanically. To obtain the semiconductor flake used in the experiments of Figure 5, the PTAA semiconductor was drop-casted onto a polydimethylsiloxane (PDMS) stamp, dried in a nitrogen environment and subsequently exfoliated with a pair of tweezers.

The XPS measurements have been carried out in a Quantera from ULVAC-PHI (Q2). The angle between the axis of the analyser and the sample surface was 51° . The measurements have been performed using monochromatic $\text{AlK}\alpha$ radiation using a spot size $100 \mu\text{m}$ (25W). By means of wide-scan measurements the elements present at the surface have been identified. Narrow-scan measurements have been performed for quantification and to determine the chemical bonding state of the elements. Apparent surface concentrations were obtained by quantification of the peak areas.

Scanning Kelvin probe microscopy measurements were performed with a Veeco Dimension 3100 AFM. First, the height profile was recorded in tapping mode. Then the potential profiles were measured in non-contact lift mode at a height of 25 nm above the surface.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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