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COMMUNICATION

Single-Layer Pentacene Field-Effect Transistors Using Electrodes Modified With Self-assembled Monolayers

By *Kamal Asadi, Yu Wu, Fatemeh Gholamrezaie, Petra Rudolf,* and *Paul W. M. Blom**

Dedicated to the memory of Prof. Bert de Boer who passed away in January 2009.

Organic field-effect transistors (OFETs) have a considerable potential for cheap disposable electronic products.[1–3] It is advantageous for circuits based on OFETs to deposit and pattern the source and drain electrodes lithographically on the gate insulator prior to semiconductor deposition in a so-called bottom-contact/bottom-gate (BC/BG) geometry. Direct access to the conducting channel, i.e., the first few nanometers in the proximity of the gate dielectric, is vital for applications such as sensing, where changes in the OFET electrical characteristics are detected due to physical/chemical interactions between the semiconductor and the analyte.[4] For such applications, a very thin semiconductor layer of only few nanometers thick with high crystallinity hence high mobility in a BC/BG structure is desired. A model system of a high mobility organic semiconductor used in OFETs is pentacene ($C_{22}H_{14}$). The charge transport properties strongly depend on the packing and orientation of the pentacene molecules,[5] which are governed in thin films as used in OFETs by the interaction between the pentacene molecules as well as their interaction with the substrate. When pentacene is deposited on SiO_2 the interaction between the pentacene molecules results in pentacene layers with an upstanding orientation, packed in a herringbone-like structure.[5] With optimized material purification,[3] deposition conditions,[1,2] and substrate treatments hole mobilities of $3\,cm^2\,V^{-1}\,s^{-1}$ have been achieved in pentacene OFETs.[6] However, these high mobilities were obtained in BG transistors by evaporating the source and drain electrodes via a shadow mask on top of the pentacene layer: the so-called top contact, bottom gate OFETs.

Unfortunately for OFET circuits based on BC/BG a fundamental problem arises: on top of the metal electrodes pentacene growth is disrupted, leading to an orientation where the pentacene molecules are lying flat on the metal surface.[5] This leads to formation of pentacene domains with varying molecular orientation, which is detrimental for the OFET performance.[5] Therefore, the OFET geometries that can be used to exploit the high mobility of pentacene are limited.[7–9] Furthermore, as a result of direct evaporation of pentacene on top of metal surfaces, an interfacial dipole (ID) appears at the metal/pentacene interface[10] which shifts the metal's work function most often to undesirable values and reflects itself in the deteriorated FET performance.[11,12]

It has been shown that assembling an array of small polar molecules that readily forms a monolayer on surfaces of metals and/or oxides allows for engineering of the metal's work function and surface energies.[13] While modification of work function[14–18] has shown to be beneficial for better performance in organic diodes,[18,19] in OFETs interface engineering has been focused on the gate oxide.[6,20] In OFETs fabricated with carbon nanotubes[21] or amorphous polymer semiconductors,[22] modifying the work function of the electrodes with self-assembled monolayers (SAMs) has been shown to influence the OFET performance. In case of pentacene- (or in general crystalline organic semiconductors-) based OFETs with SAM-modified gate oxide and/or electrodes, however, changes in performance are accompanied by changes in the morphology of pentacene (or crystalline organic semiconductor) deposited onto the modified surface.[23–25] Recent studies on metal/SAM/pentacene systems have shown that SAMs not only alter the alignment of the electronic energy levels at the interface, but also influence the morphology of the evaporated pentacene layers.[26–29] The presence of the SAM on the metal reduces the surface free energy and promotes the growth of pentacene layers with a standing-up orientation.[30] In this respect, understanding of the SAM-modified electrodes in OFETs becomes complex when both interfacial energetics and morphology are simultaneously changed. In this communication, in order to reach a conclusive understanding on the role of the SAM, we disentangle the alignment of the energy levels at the interface from the morphology. To this end, we used bare silicon oxide (without any further treatments) as the gate dielectric throughout the experiments which served as the reference morphology and we then studied the morphology at the electrode/gate oxide interface. The gold electrodes were modified with a monolayer of molecules having opposite dipoles moments which were applied by self-assembly. Then we address which of the two, i.e., aligned energy levels or morphology, has a more pronounced influence on the OFET performance in a BC/BG geometry. We demonstrate that the interfacial morphology between the SAM-modified contacts and the transistor channel dominates the FET performance rather than manipulation of the Schottky barrier and charge injection. The SAM-modified electrodes enabled us to

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control the morphology to such an extent that stable and reproducible BC/BG OFETs with only one monolayer of pentacene as the active semiconducting material were realized.

Pentacene ultra-thin film growth was carried out by a supersonic molecular beam deposition technique (SuMBD). Since the first few monolayers and their corresponding morphology in the proximity of the electrodes and on the gate insulator dominate the OFET performance, experiments were carried out with ultra-thin pentacene films of only one or several monolayers (ML). High crystallinity in the pentacene was achieved by carrying out the SuMBD at a kinetic energy of 6.4 eV.[31] Reference morphology analysis were performed by examination of monolayers deposited on bare silicon oxide using ex situ tapping mode atomic force microscopy (AFM) and X-ray diffraction (XRD). Prior to the deposition of pentacene on the FET substrates, the lithographically patterned gold source and drain electrodes on a standard heavily doped Si substrate with a 250 nm SiO_2 gate insulator, were covered with SAMs of thiols with opposing dipole moments. These monolayers enable the modification of the work function of the gold source and drain electrodes in opposite directions.[18,22] The electrical measurements on the pentacene OFETs were performed in high vacuum, after which the pentacene surface morphology was characterized by AFM.

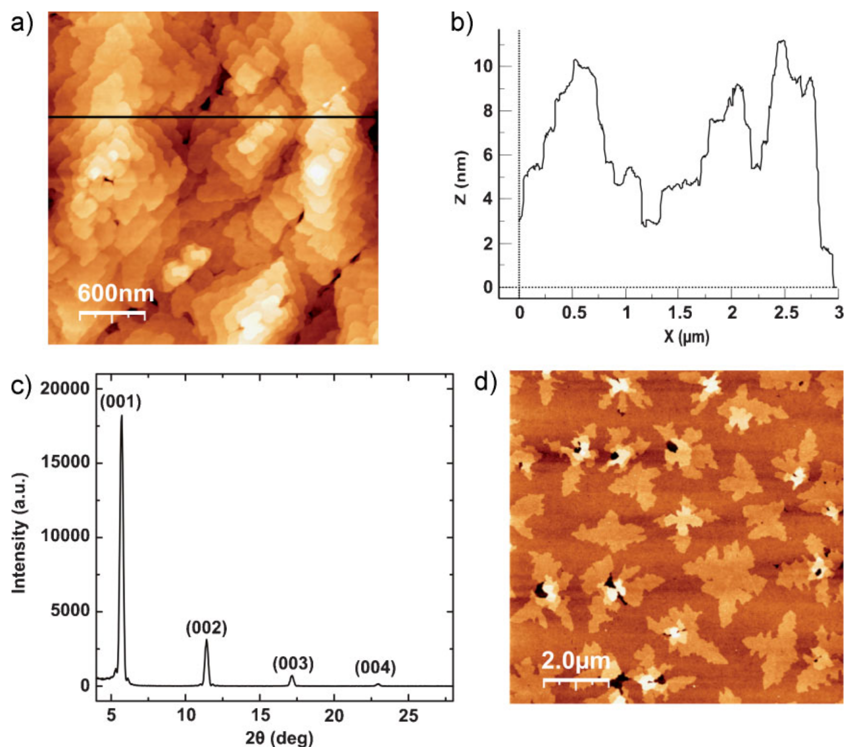

Figure 1. Reference AFM images of pentacene ultra-thin films grown on bare silicon oxide surface: a) AFM height image of pentacene (3 µm × 3 µm) with nominal thickness of 6 ML of pentacene. b) The line profile of the height image of (a) which shows that under this condition only the first two layers are completed. c) XRD of 6 ML pentacene film prepared at the optimum SuMBD conditions demonstrate a highly crystalline film. d) AFM height image (10 µm × 10 µm) of pentacene ultra-thin film with nominal thickness of 1.3 ML showing a completed first monolayer followed by initiation of the growth of the over layers. The first monolayer acts as a perfect template for growth of the over layers.

The reference morphology of pentacene ultra-thin films deposited by SuMBD with a nominal thickness of 6 ML is shown in Figure 1a, where after completion of the first monolayers typical island growth is observed. We estimate from the line profile of the surface of the Figure 1b that only 2 ML above the SiO_2 surface are completed. The molecular islands formed in each layer mimic exactly the geometrical shape of the larger islands underneath.[31] Pentacene islands in Figure 1a signify the typical crystal facets with regular geometric shape with very sharp and straight island edges. This implies a homoepitaxial-like growth among the intra-pentacene layers. Characterizing the crystal structure with XRD (Fig. 1c) showed four very sharp, narrow diffraction peaks with high intensity that correspond to the (00*l*) indexes. Based on Bragg's law, a lattice parameter of ~15.5 Å is extracted in agreement to the previous reports.[32–34] In the detailed structure of (001) diffraction peak, two different phases appear to the right of (001) with inter-plane distance of ~14.4 Å corresponding to the (001) single crystal phase[35,36] and to the left of (001) with inter-plane distance of ~16.4 Å corresponding to a configuration in which pentacene molecules stand up at 90° angle with respect to the substrate surface.[37] These phases however, make up a very small fraction of the film, as evidenced by their extremely low X-ray diffraction intensity. Since there is no indication of other polymorphs, this suggests a uniform crystal structure of ultra-thin film of pentacene. Due to the compact island structure, the internal crystal defects were reduced and a thin film of pentacene with high crystallinity was obtained.

The uniform crystallinity of the pentacene film originates from the perfect first pentacene monolayer. The reference morphology measurement for an ultra-thin pentacene film grown on bare silicon oxide with nominal thicknesses of 1.3 ML is presented in Figure 1d. The height image of Figure 1d after deposition of 1.3 ML demonstrated the formation of a completely closed first monolayer, followed by the initiation of the second monolayer which is stopped at a coverage of ~30%, thus consistent with the layer-by-layer growth mode.[38]

To explore the role of the SAMs on aligned energy levels at the interface we carried out experiments where the gold electrodes were treated with SAMs of opposite dipoles namely, 1*H*,1*H*,2*H*,2*H*-perfluoro octanethiol (PFOT) and decanethiol (DT). Kelvin probe measurement showed that PFOT and DT change the work function of gold from 4.8 eV to 5.5 and 4.2 eV, respectively.[18,22] After the treatment of the gold source and drain electrodes with the appropriate SAM (PFOT or DT), pentacene with nominal thickness of only 6 ML is deposited on the modified FET substrates. The output characteristics (Fig. 2a) of both of the SAM-modified FETs show decent current amplification, contrary to the device with untreated gold electrodes. Transfer characteristics of the FETs are given in Figure 2b. FETs with PFOT or DT

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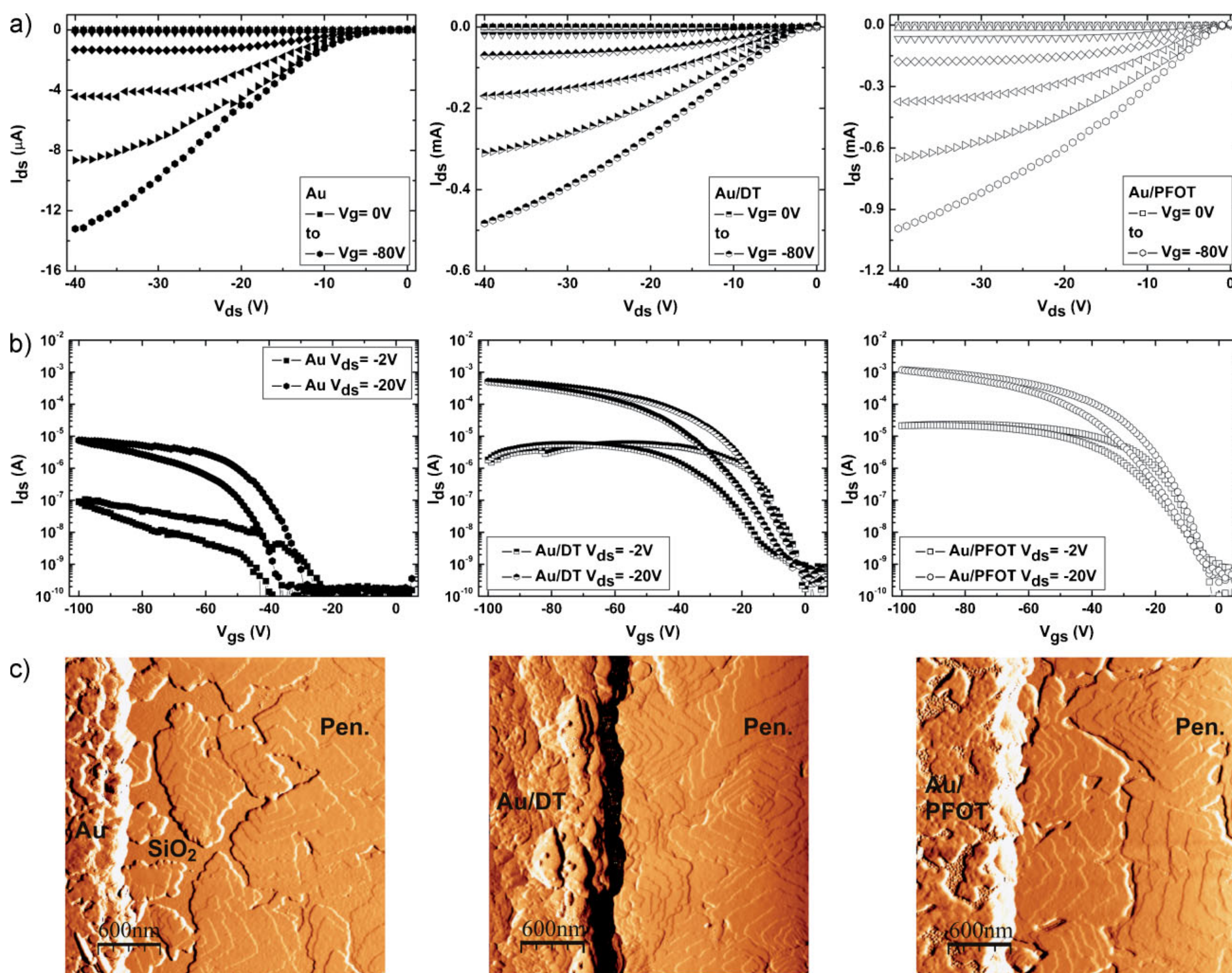

Figure 2. a) Output characteristics of typical OFETs with Au electrode (left), Au/DT (middle) and Au/PFOT (right). b) Transfer characteristics of the same FETs. The OFETs with modified Au electrodes display almost zero switch-on voltage and a very high mobility. All transistors in (a) and (b) have the same channel length/channel width of 20/10 000 and an oxide thickness of 250 nm. c) AFM amplitude images (3 μm × 3 μm) of pentacene ultra-thin films with nominal thickness of 6 ML. Images recorded at the border between the (modified) gold electrode and silicon oxide surface covered with pentacene.

treated electrodes, exhibit a superior performance compared to their untreated counterpart. The device current in the saturated regime for the SAM-modified OFETs is more than two orders of magnitude higher, the on/off ratio is typically 10^6 and the mobility was determined to be 0.02–0.05 $cm^2\ V^{-1}\ s^{-1}$ in the saturation regime. For the unmodified device, however, the mobility is typically two orders of magnitude lower. We note that pentacene mobilities $>1\ cm^2\ V^{-1}\ s^{-1}$ are only obtained in BG transistors with vapor-deposited top contacts and an octadecyltrichlorosilane (OTS) or hexamethyldisilazane (HMDS) treated SiO_2 surface.[6] To distinguish the effects of SiO_2 treatment from the effect induced by modification of the electrode we deliberately used bare SiO_2 in this study, leading to lower carrier mobilities.[6,20,39] Another remarkable feature of the SAM treatment of the electrodes is strong decrease in the switch-on voltage of the corresponding FETs whereas this effect is usually attributed to the trapped charges at the gate insulator/semiconductor interface.

Justifying the enhanced performance of the SAM-modified OFETs with better-aligned electronic energy levels at the contacts is clearly inconsistent with the measurements. From the work function measurement, it is expected that Au/PFOT/pentacene gives rise to an Ohmic contact, while the Au/DT/pentacene is expected to have a large energy offset with a charge injection barrier of ∼0.7 eV.[40] The latter is anticipated to have a limited charge injection and, therefore, an inferior performance. Nevertheless, the electrical characteristics of the OFET with Au/PFOT and Au/DT as electrodes are comparable. Additionally, SAMs influence the morphology by changing the surface energy dramatically. Thus, we studied the correlation between morphology and performance of the untreated and SAM-modified pentacene OFETs. Two scan regions of interest were selected: i) in the middle of the transistor channel (away from the gold electrode); and ii) at the boundary between electrode and the channel to inspect the morphology on the silicon oxide gate insulator and the electrode/channel interface, respectively. Height and amplitude images were simultaneously recorded for each sample. We adapted the amplitude image to present our data since it can provide a very high topographic resolution even for a rather complex surface. The height image resolution is cloaked due to the large surface height difference at the border

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between the gold electrode (~150 nm thick) and the silicon oxide. The surface morphology in the middle of the channel for all transistors resembles exactly that of the reference morphology for 6 ML of pentacene on pristine silicon oxide given in Figure 1a–c. This implies that we have the same growth conditions and the same film morphology and hence crystallinity. Moreover, it shows that the growth in the middle of channel is not influenced by the presence of the gold–pentacene interactions. However, the difference in morphology between the untreated and SAM-modified gold electrode at the gold electrode/SiO_2 boundary is striking. The homoepitaxial-like growth among the intra-pentacene layers is disrupted and the crystallinity of the film is discontinuous in the vicinity of the bare gold electrode (Fig. 2c). Here, separated sub-micron size 3D clusters of small aggregated pentacene grains are observed and the exposed silicon oxide surfaces without any pentacene are still visible. This clearly shows that the presence of the gold electrodes affects the growth of pentacene, leading to a morphological transition regime with an average width of about 1 μm. The fact that the pentacene molecules adopt a flat-lying structure on gold, and up-standing orientation on silicon oxide, causes formation of this region during the deposition with small grains and many grain boundaries. Field-effect transistors with SAM-modified source–drain electrodes were also analyzed by AFM. The morphology on the silicon oxide far away from the electrodes is again identical to the reference morphology, as depicted in Figure 1a–c. The AFM images at the boundary between the Au/DT as well as the Au/PFOT electrode and the silicon oxide demonstrate that the surface morphology of the pentacene film is continuous (standing-up) and extends from the channel directly till to the edge of the electrodes (Fig. 2c). Moreover, the morphological transition region near the electrodes is completely eliminated and interfaces with highly uniform morphology and very large crystal terrace have been successfully obtained at the edge of the SAM-modified gold electrodes and silicon oxide. It is evident that the difference in morphology between the untreated and SAM-modified Au electrodes severely affects the electrical performance of the OFETs (Fig. 2a left panel vs. Fig. 2a middle and right panel). The presence of which explains the occurrence of high resistances in transistors with small channel lengths.

These electrical measurement combined with the morphological analysis revealed that the SAM-modified gold electrodes (modified by both PFOT and DT) predominantly influence the growth of the pentacene film at the vicinity of the contacts and the improved morphology results in an enhanced electrical performance rather than the alignment of the energy levels at the contact and manipulation of the injection barrier.

We note that in pentacene films with nominal thickness of 6 ML used in our experiments, only the first two monolayers were continuous and fully completed (Fig. 1a and b). Observation of this continuous morphology of the pentacene film at the edges of the Au/SAM electrodes as in the middle of the channel, leads us to assume that our SAM-modified BC/BG transistor substrates are first covered with a continuous pentacene monolayer. This first monolayer exhibits a good crystallinity and homogeneity over the complete substrate onto which the growth of the next layers was initiated.

To test our assumption only 1 ML of pentacene was deposited on the transistor substrates with bare gold electrodes and with PFOT-modified gold electrodes (without any treatment of the silicon oxide). AFM analysis of the pentacene monolayer (Fig. 3A) demonstrated that the surface morphology in the middle of the channel resembles exactly that of the reference morphology for 1 ML pentacene on pristine silicon oxide as given in Figure 1d, which implies that growth in this region is not influenced by presence of the (un)modified electrodes. However, the difference in morphology at the electrode/semiconducting channel boundary is again prominent between the untreated and PFOT-modified gold electrodes. Remarkably, at the boundary between the Au/PFOT electrode and the silicon oxide the surface morphology of the pentacene monolayer is continuous and the large pentacene monolayer terraces extend from the edge of the electrodes into the channel and no morphological transition region is observed (we note that the condition used for growth of the 1 ML led to 0.9 ML hence the film does not fully cover the substrate). For the untreated gold electrode (Fig. 3a), the morphological transition regime was formed at the boundary of the Au electrode/SiO_2 interface and no large pentacene monolayer terraces are observed. The electrical output characteristics of the two OFETs (Fig. 3b) show that the transistor with the unmodified Au electrodes hardly turns on and very low currents are observed (nA), while the PFOT-modified transistor illustrates very good field-effect characteristics with high currents of μA. By modifying the Au electrode with a single monolayer of PFOT, the drain currents obtained are more than three orders of magnitude higher over the complete bias range. Further investigation of the transfer characteristics of the FETs (Fig. 3c) demonstrates that the unmodified transistor displays a large switch-on voltage of around −60 V, a low on/off ratio, and a very low saturated current. Consequently, the mobility amounts to values of only 10^{-5} cm^2 V^{-1} s^{-1} in the saturation regime.

However, the monolayer pentacene OFETs with PFOT treated electrodes exhibit a superior performance compare to its untreated counterpart. The FET current in the saturated regime is three orders of magnitude higher with large on/off ratio and charge carrier mobility that amounts to 0.015 cm^2 V^{-1} s^{-1}. The current is free of hysteresis and the switch-on voltage is shifted to −10 V. PFOT treatment of the electrodes has a significant effect on the switch-on voltage and strongly reduces the hysteresis. These effects are usually attributed to trapped charges at the gate insulator/semiconductor interface. Nevertheless the occurrence of a discontinuous transition region and small pentacene islands can explain also the hysteresis in the transfer characteristics. Injected charges are trapped at the grain boundaries of the pentacene islands in the case of OFETs with untreated electrode leading to hysteresis and high switch-on voltage. In contrast, the monolayer pentacene OFETs with the SAM-modified electrode demonstrates a highly uniform morphology at the edge of the SAM-modified electrode/silicon oxide. Therefore, the transition regime is eliminated and less traps are expected, hence a low switch-on voltage and less hysteresis. The realization of an efficient BC/BG transistor with only 1 ML of pentacene that has been elusive so far can be achieved by simply inserting a monolayer of PFOT on the gold electrode. This technique resolves the scaling issues inherited from the shadow mask techniques for evaporation of top source and drain electrodes on the semiconductor and opens a new route to realization of high crystalline films in BC/BG transistors.

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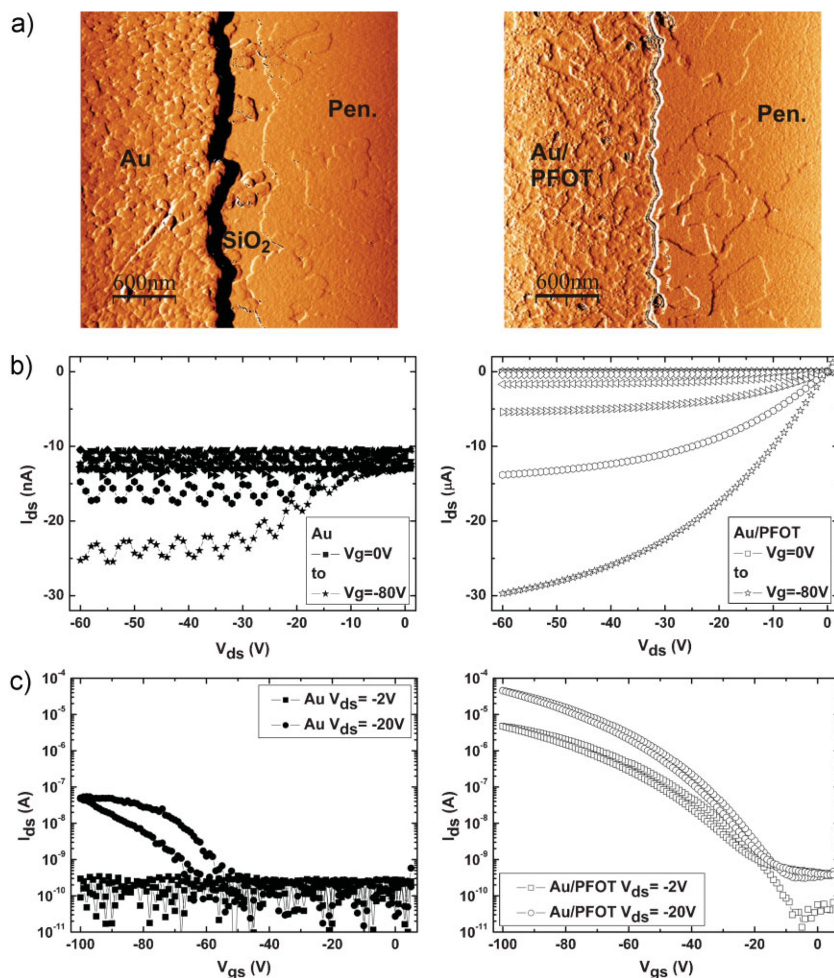

Figure 3. a) AFM amplitude images (3 μm × 3 μm) of a monolayer of pentacene at the interface between the gold electrode and the silicon oxide surface where the left image depicts a pentacene monolayer grown next to the bare gold electrode and the right image shows a pentacene monolayer grown next to the PFOT-modified gold electrode. b) Output characteristics of transistors with Au (left) and Au/PFOT (right) electrodes. Note that the y-axis is adjusted from nA to μA. c) Transfer characteristics of the same transistors as in (b) with Au (left) and Au/PFOT (right) electrodes showing the superior performance of the Au/PFOT monolayer pentacene OFET. All the transistors have a channel length/channel width of 10/10 000 and an oxide thickness of 250 nm.

Modifying the SiO_2 toward achieving high mobilities is the next step to optimize the 1 ML OFET even further and make it more appealing for future applications. Furthermore, the results of the experiments presented here gives the opportunity to directly access the conducting channel of the field-effect transistor which is highly appreciated for sensing applications.

In conclusion, we have demonstrated that the performance of pentacene OFETs is improved by modifying the metal electrodes with SAMs. The dominating role on the performance is played by the morphology of pentacene rather than the aligned energy levels at the contact. The preferred orientation of the pentacene on and next to the SAM-modified metal electrodes is identical to the orientation of the pentacene on SiO_2, and, therefore, no small crystalline domains are found near the SAM-modified electrodes. Due to the absence of small crystallites, pentacene grain boundaries are eliminated and charge trapping hardly occurs which led to good field-effect behavior of the transistors without a large switch-on voltage. With optimized growth condition of pentacene on the substrates via the supersonic molecular beam deposition, hysteresis-free transfer curves with very small switch-on voltages were obtained even for only a single monolayer of pentacene as active channel. The new insights on how to realize OFETs with electrically stable contacts and only one monolayer of 1.5 nm as the active semiconductor in the channel, paves the way toward future exotic applications such as sensors based on OFET.

Experimental

For AFM imaging of the reference morphology, the surface of the silicon substrates were cleaned with acetone to remove any traces of contamination and were subsequently subjected to UV–Ozone cleaning for 20 min. A homemade SuMBD was used to grow pentacene ultra-thin films with optimized growth condition for the high quality ultra-thin pentacene film, i.e., a kinetic energy of 6.4 eV [41,42]. The supersonic molecular beam with high directionality and narrow angular distribution was introduced into the deposition chamber for pentacene growth. The deposition was carried out by impinge the incoming molecular beam on the substrate surface at a normal incidence angle at room temperature and a constant chamber pressure of 1.7×10^{-7} mbar. A very low growth rate of $\sim$0.4 Å min^{-1}, monitored by the quartz crystal microbalance and calibrated by the AFM thickness measurement, was used. The first pentacene monolayer on SiO_2 was completed after 50 min of deposition. The morphology of the films was studied by using ex situ tapping mode AFM (Digital Instruments). The AFM height and amplitude images were simultaneously recorded at room temperature under ambient conditions after the electronic measurement. The AFM images of 10 μm × 10 μm and 3 μm × 3 μm were recorded with a resolution of 512 × 512. FET substrates were fabricated using conventional lithography and obtained from Philips Research Laboratories (Eindhoven, The Netherlands). Thermally grown silicon oxide (250 nm) was used as the gate insulator. Using conventional lithography, gold source and drain contacts were patterned with finger geometry with 5 nm of titanium as adhesion layer. The channel length varied from 4 to 40 μm while the channel width was kept constant at 10 000 μm. The FET substrates were dipped in a Piranha solution (demi water 100 mL + ammonia (30%) 20 mL + H_2O_2 20 mL) for 60 s at 70 °C to remove all organic impurities from the surface of metal as well as from the oxide. Then the substrates were submerged in acetone in an ultrasonic bath for 5 min and spin dried. Next the substrates were UV–Ozone cleaned for 20 min. For the self-assembly process, (perfluoro)alkanethiols [18] were dissolved in ethanol ($\sim$1–3 × 10^{-3} M). The FET substrates were immersed in the SAMs solution over night. After the self-assembly process, the substrates were thoroughly rinsed with ethanol, toluene, and 2-propanol,

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dried with a deionized N_2 flow. Pentacene was deposited using the optimum SuMBD condition, i.e., at a kinetic energy of 6.4 eV. Electrical measurements were carried out in a homebuilt probe station under high vacuum (10^{-6} mbar) with a Keithley 4200 semiconductor analyzer at room temperature, after which the surface morphology was analyzed by AFM.

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