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Evidence for Thermal-Based Transition in Super-Lattice Phase Change Memory

Mattia Boniardi,* Jos E. Boschker, Jamo Momand, Bart J. Kooi, Andrea Redaelli, and Raffaella Calarco

Phase change memory (PCM) device physics comprehension represents an important chapter of future development of the PCM-based architectures and their placement into the storage class memory (SCM) segment of the memory hierarchy. Here, a reduction of SET and RESET currents by more than 60% with respect to conventional GeTe–Sb₂Te₃ (GST) alloys is demonstrated by using phase change memory cells containing (GeTe–Sb₂Te₃)/Sb₂Te₃ super-lattices (SL). Further, it is demonstrated that our SL PCM devices have similar characteristics in terms of the memory transition as conventional memory cells based on GST, even though showing reduced power consumption, indicative of an efficiency augmented SET-to-RESET transition. The reduced power consumption may be attributed to an increased thermal resistance of the SL with respect to the bulk GST alloy. This demonstrates that it is possible to engineer PCM with enhanced performance by employing SL structures, enlarging the possibility of employing SL as SCM players.

Phase change memory (PCM) based technologies show the characteristics to become players in the future non-volatile memory market.^[1–4] The PCM technology relies on the reversible transition between the high resistance amorphous phase (RESET state) and low resistance poly-crystalline phase (SET state) of phase change materials, such as GeTe–Sb₂Te₃ (GST) alloys. The strong contrast in the resistivity of both phases, in the range 10²–10³, allows for the electrical determination of the phase of the memory element and thus the readout of the stored data. One of the main opportunities in PCM is the research and development of materials, proper active stacks and/or architectures to reduce the power consumption required for

the RESET operation, namely the electrical power needed for melting the active core of the phase change material. For example, the power consumption can be reduced significantly by down scaling the devices and $I_{\text{RESET}} = 5 \mu\text{A}$ writing current has been demonstrated by using carbon nanotube electrodes.^[5] However, device dimensions are dictated by the current technology node and in the recent years a number of new PCM device concepts have been introduced in order to improve the power consumption and thus the device performance. For example, Ahn et al.^[6] demonstrated that the RESET current of PCM device could be reduced by 40% when a graphene layer was introduced between the Ge₂Sb₂Te₅ phase change material and the W bottom contact. This was attributed to an improved thermal energy management in such devices. Another approach to reduce the power consumption is the use of super-lattices

(SLs) as active materials.^[7–20] Chong et al.^[7] ascribed this reduction to an improved heat management in SL-based devices and Tong et al.^[8] further support this picture thanks to thermal conductivity measurements using the 3 ω method on SL chalcogenide materials, compared to some bulk materials. They propose a *phonon mode vanishing* description, based on phonon–interface interactions, to explain the lower thermal conductivity of the SL stack. On the same context, Long et al.^[9] report extensive calculations of the phonon properties of some chalcogenide stacks, pointing out that a low phonon group velocity and the thermal resistance at interfaces result in a low thermal conductivity of the GeTe/Sb₂Te₃ SL material, making it the best choice for phase change memory. Simpson et al.^[10] on the other hand measured an increased thermal conductivity in GeTe/Sb₂Te₃ SL and concluded that the programming current was not reduced by an improved heat management. Instead they invoke a non-thermal switching of Ge atoms,^[10] possibly caused by charge injection^[11,12] or electric fields.^[13] Advanced density functional theory calculations indeed show that atomic switching is possible by a two-step process.^[14] More recently it was reported that biaxial strain in GeTe/Sb₂Te₃ SL can lead to enhanced diffusive atomic disordering within the GeTe layers, eventually resulting into higher atomic switching probability in the pre-melting temperature range of GeTe and below the melting temperature of Sb₂Te₃.^[15] Recent scanning transmission electron microscopy (STEM), extended X-ray absorption

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fine structure (EXAFS), and X-ray diffraction (XRD) investigations of epitaxial GeTe/Sb₂Te₃ SLs grown by molecular beam epitaxy (MBE) revealed, however, that GST phases are formed in such SLs, questioning the atomic displacement picture.^[16–18] Moreover, it was found that such SLs are thermodynamically unstable and transform into GeTe-Sb₂Te₃ alloys upon heating.^[16] Recently, another study based on first principles calculations on intermixed GST/Sb₂Te₃ SL claimed that a stacking-fault motion can alter the bandgap by breaking the local chemical stoichiometry and can result in a reversible metal-insulator transition.^[19] Finally, a conceptually novel mechanism, based on the inversion of SbTe bilayers and the subsequent reconfiguration of van der Waals (vdW) gaps,^[20] has been proposed and highlighted not to be compromised by Ge/Sb intermixing. Despite many theoretical studies in the literature propose different mechanisms to explain the SL transition, sometimes supported by a thermal-based picture, sometimes not, a detailed analysis of the transition between the electrical SET and RESET states in SL-based PCM devices is still lacking and is clearly needed with the aim of inferring possible characteristics of the transition and, eventually, to allow the control of such devices and to make them attractive for industrial development.

To increase our understanding of SL-based devices, GeTe/Sb₂Te₃ SLs were grown on top of PCM device structures and planar substrates by MBE as described in the Experimental Section. The deposition of phase change materials at elevated temperatures on the device structure normally results in polycrystalline films, due to the amorphous nature of the device structure (the bottom electrode contact and the surrounding dielectrics).^[21] However, the two-dimensional (2D) nature of Sb₂Te₃ makes it possible to obtain a (0 0 0 1) texture.^[10,22,23] **Figure 1** shows the structural characterization of SLs grown on the device structure and on amorphous substrates. The

reflection high-energy electron diffraction (RHEED) pattern taken directly after the deposition, Figure 1(a), shows clear strikes, in good agreement with a (0 0 0 1) texture of the SL. Furthermore, investigation of the surface of the final device using scanning electron microscopy (SEM), i.e., Figure 1(b), reveals that the surface is flat, which is not the case for polycrystalline films.^[21] The (0 0 0 1) out-of-plane orientation of the SL is also clearly observed using high resolution TEM. Figure 1(c) shows a representative cross-sectional TEM image of a SL grown on a plain amorphous substrate using the same conditions as for the device fabrication. In the image one can clearly observe dark lines that are parallel to the interface between the substrate and the SL that is indicated by the dotted white line. Such dark lines are caused by the presence of vdW gaps in 2D-bonded materials.^[22] In Sb₂Te₃ the distance between the vdW gaps is ≈ 1 nm, whereas it is larger for GST phases. The distance between these lines can thus be used to identify the phases in the SL. The thickness of the first five layers, marked by the upward pointing arrows, is determined to be 1 nm, consistent with the layer thickness of Sb₂Te₃. The subsequent two layers have a thickness of ≈ 1.3 nm, which is consistent with the layer thickness of GeSb₂Te₄.^[24] A precise determination of the total stacking sequences is not possible, but additional Sb₂Te₃ and GST phase can be recognized in the remainder of the SL and are marked with arrows. We note that the observation of GST phases in this kind of SLs is in full agreement with previous investigations of epitaxial SLs.^[16–18] Hence, the SL is a GST/Sb₂Te₃ SL even though alternating layers of GeTe and Sb₂Te₃ were grown. The XRD characterization of the SL grown on the device structure, i.e., Figure 1(d), is consistent with this interpretation. The XRD profile shows a strong zeroth order diffraction peak at $3.66 \text{ \AA}^{-1}$ and a broad feature around $3.2 \text{ \AA}^{-1}$. The broad feature can be attributed to the diffraction peak

Figure 1. a) RHEED pattern taken after the deposition of the SL on the device structure. The streaky pattern is typical for a two-dimensional surface of a (0 0 0 1)-oriented SL with a random in-plane orientation. b) SEM image of the surface of a device structure after deposition of the W top electrode, showing a low surface roughness. c) HRTEM image of a SL on a plain amorphous substrate. The (0 0 0 1) out-of-plane orientation and the alternating layers of Sb₂Te₃ and GST can easily be recognized. d) XRD profile of a SL grown on the device structure. The diffraction peaks corresponding to Sb₂Te₃, GST and the SL are marked accordingly.

originating from the presence of Sb_2Te_3 and GST in the SL^[18] and thus confirms that the SL grown on the device structure is a GST/ Sb_2Te_3 SL, from now on, SL. Such a SL stack, featuring thickness $t_{\text{SL}} = 45 \text{ nm}$, has been deposited in a test structure with a 2500 nm^2 contact area between the bottom electrode contact (BEC) and the chalcogenide SL. The stack has been eventually capped with a 50 nm thick tungsten (W) cap, acting as top electrode contact (TEC). The SL samples have been electrically characterized by collecting the programming curves (R – I) and the pulsed characteristic curves (I – V), with the instrumentation described in the Experimental Section and the results are reported in **Figure 2**. A pulse duration $T = 300 \text{ ns}$ was adopted in order to be able to obtain a significantly high amount of points for current readout within the pulse time domain. In principle, a pulse as short as possible can be used to safely catch the SET-to-RESET transition, whereas $T > 200 \text{ ns}$ is considered safe to entirely catch the RESET-to-SET transition. On the same cell vehicle, a bulk $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST) was grown by MBE as well, with thickness $t_{\text{BULK}} = 70 \text{ nm}$, and characterized for reference. Figure 2a reports the R – I curves of both the bulk GST and SL devices: the measured samples show qualitatively similar R – I

curves, but a strong reduction in the RESET current of the SL-based device, from $I_{\text{RESET}} = 1\text{--}1.5 \text{ mA}$ for bulk GST, down to $I_{\text{RESET}} = 0.4\text{--}0.5 \text{ mA}$ for SL, revealing a RESET current reduction of a factor 3. Such current reduction in the SL device would not be expected in a conventional PCM framework with comparable thermal properties of the stacks: in fact, the thickness of the active layers is different, $t_{\text{SL}} < t_{\text{BULK}}$, leading to a higher current expectation in SL, than bulk, owing to closer thermal boundaries from the BEC and the TEC in the SL case.^[28] Hence, the reported current reduction for the SL case is to be considered as a strong evidence of an optimized stack in terms of its thermal properties and/or of a SET-to-RESET transition mechanism with much higher efficiency than the bulk counterpart. Further, it is worth to notice that the SET state resistances in Figure 2a are pretty aligned between the two cases and the very negligible displacement in terms of R_{SET} is not enough to justify the strong current reduction reported for the SL case, as will be discussed below. Moreover, the RESET resistance level in Figure 2a is reported to be higher for the SL case, than the bulk GST, of about a factor 8. Such discrepancy, with the additional feature of a much steeper SET-to-RESET edge in the SL case, can be ascribed to different material response to electrical stress occurring in the two cases. In fact, bulk GST may be more prone to feature ion migration during the programming operation due to the absence of physical barriers (e.g., vdW gaps) preventing elemental motion by wind force and/or an applied electric field and/or a thermal gradient.^[25] For this reason, bulk GST may feature an antimony rich region (Sb-rich GST) in the active volume,^[26] translating into a higher electrical conductivity of the RESET state due to the metallic-like behavior of antimony.^[27] On the other hand, the presence of the vdW gaps in the SL stack, discussed in Figure 1, could strongly limit such ionic migration, resulting into a higher RESET state resistance and into a much steeper SET-to-RESET transition, consistent with a less/non Sb-enriched phase. In this context, the RESET state relies on an amorphous, bulky phase for bulk GST, whereas it is the result of amorphous stripes delimited by the vdW gaps in the SL case, in which stripes are represented by the intermixed regions of the SL. Figure 2b reports the pulsed I – V curves of the two cases: the characteristic curves are shown to be qualitatively similar for both the SET and the RESET state: the RESET I – V curves show a threshold switching behavior and the ON-state regime is qualitatively aligned in the two cases. From the quantitative standpoint, bulk GST shows a very slightly higher threshold switching voltage with respect to SL, with $\Delta V_{\text{TH}} = 100 \text{ mV}$. The presence of a similar threshold switching voltage, V_{TH} , in both SL and bulk GST is pointed out here as a possible signature of the presence of an amorphous phase within the active material. A reported lower V_{TH} in the SL case can be ascribed to an overall thinner layer, in terms of the thickness of the film and as a result of the stacking of multiple thin and amorphous GST layers, separated by vdW gaps and by the Sb_2Te_3 layers. We also note that this represents a reasonable possibility and no clear threshold switching behavior has been reported for SL devices ever. The ON-state differential resistance can be extracted from the slope of the I – V curves in the ON-state regime, shown in Figure 2b. The determined values are $R_{\text{ON}} = 400 \Omega$ for bulk GST and $R_{\text{ON}} = 440 \Omega$ for the SL. The ON-state resistance computation allows to directly translate

Figure 2. Resistance as a function of an increasing programming current, I_{PROG} , starting from the SET and from the RESET state for bulk GST and SL, showing that the RESET state can be obtained by currents in the range of $400\text{--}500 \mu\text{A}$ and $1\text{--}1.5 \text{ mA}$ in SL and bulk GST, respectively (a); I – V characteristic curves, resulting scaled, accordingly with currents (b). The inset reports a sketch of the cell vehicle.

the current reduction factor introduced above into a power reduction factor: in fact, as $P_{\text{RESET}} = R_{\text{ON}} I_{\text{RESET}}^2$, the RESET power can be computed as $P_{\text{RESET}} = 0.9 \text{ mW}$ for bulk GST and $P_{\text{RESET}} = 110 \mu\text{W}$ for SL, that is a rough power dissipation reduction $f_p \approx 9$, to obtain the RESET state, as expected from the $P-I^2$ proportionality law and the reduction of the programming current by a factor $f_i \approx 3$. The electrical power to be injected to have the first raise of resistance in the $R-I$ curves (melting power in conventional PCM), can be computed as well, leading to $P_{\text{BULK}} = 170 \mu\text{W}$ and $P_{\text{SL}} = 20 \mu\text{W}$ for bulk GST and SL, respectively. It should be stressed that the presence of an intermixed phase, leading to a $\text{Sb}_2\text{Te}_3/\text{GST}$ SL, the presence of a threshold switching voltage, related to the RESET state of SL, close to the value of the bulk counterpart, the presence of a higher RESET/SET resistance ratio and the much steeper SET-to-RESET transition for SL, than bulk GST, can be consistent with a conventional, thermal driven, phase change mechanism occurring in the GST layers of the SL stack, as in bulk GST. The power dissipation reduction should be ascribed to a strongly augmented, stack-related, efficiency in SL.^[7]

Moreover, data coming from multiple devices characterization, including poly-crystalline GST, textured GST and SL, are collected in an $I_{\text{RESET}}-R_{\text{SET}}$ plot,^[28] as reported in **Figure 3**. Bulk GST has been obtained by the poly-crystalline and the textured depositions: the former ends up with a poly-crystalline structure as in ref. [21]; the latter ends up with an ordered structure, thanks to a tight control of the MBE deposition parameters. It is worth noticing, first, that bulk GST (poly-crystalline and textured) and SL data points cover approximately the same range in terms of R_{SET} , but with an I_{RESET} shift toward lower currents for the SL ones. Second, within such R_{SET} range, both types of devices (on one hand, poly-crystalline and textured GST; on the other hand, SL) show a reduction of the transition current with increasing

Figure 3. At constant R_{SET} , SL shows reduced current to reach the RESET state than the bulk GST counterpart, here represented by bulk and textured GST. Moreover, no significant differences can be reported between bulk GST (poly-crystalline) and textured GST (ordered structure). The thickness of bulk GST, textured GST and SL is $t_{\text{BULK}} = 70 \text{ nm}$, $t_{\text{TEXT}} = 40 \text{ nm}$, and $t_{\text{SL}} = 45 \text{ nm}$, respectively.

R_{SET} . The former relies on the SL increased efficiency, the latter could be ascribed to an area modulation effect, affecting all devices. The total I_{RESET} current reduction amounts to a factor of three and can be well described by conventional PCM equations that state $I_{\text{RESET}} \sim 1/\sqrt{R_{\text{SET}}}$.^[28] Since this equation is derived using the Fourier's law of heat transfer and is based on Joule heating, the observation of the same trend in bulk GST and SL data suggests that the SET-to-RESET transition in the SL based device also could have a thermal origin. In the case of conventional PCM working principle, a temperature raise will be mandatory and is, according to the integral of the Fourier's law of heat transfer, given by: $\Delta T = R_{\text{TH}} \cdot P$, with R_{TH} being the thermal resistance of the PCM device.^[28,29] The vertical shift in current from bulk GST downward to SL and the already commented steepness of the SET-to-RESET transition of SL is likely related to a higher thermal efficiency of the SL stack. In particular, a quantitative estimation of the efficiency difference between the two cases can be provided by supposing that in both cases melting is happening within GST, with a melting temperature, $T_{\text{MELT}} = 900 \text{ K}$. By considering a temperature–power dissipation ($T-P$) plot, a $P_{\text{MELT}} = 20 \mu\text{W}$ and $P_{\text{MELT}} = 170 \mu\text{W}$ power dissipation will occur at $T = 300 \text{ K}$ for SL and bulk GST, respectively; a $P_{\text{MELT}} = 0$, instead, will occur in both cases at $T = 900 \text{ K}$, because in this case the melting is due to the externally provided temperature.^[29] By computing the slopes, an estimation of the thermal resistance can be ruled: $R_{\text{TH}} = 29$ and $3.5 \text{ K} \mu\text{W}^{-1}$ for SL and bulk GST, respectively. The bulk GST value is in the typical range, found in the literature, for thermal resistance^[28–30]; instead, the estimated SL value results quite augmented, by a factor of 8, yet not out of range. According to this analysis, the SL stack is much more efficient in terms of heat confinement: in fact, in order to get the same ΔT , with a much less power amount ($f_p \approx 9$), the thermal resistance of SL must be quite increased with respect to bulk GST, with a device geometry tending to disadvantage the SL-based cell due to a lower active layer thickness^[28] than the bulk counterpart. Such a R_{TH} increase can be likely enabled by the multiple stacking of $\text{Sb}_2\text{Te}_3/\text{GST}$ layers and by the stack interruptions brought by the vdW gaps in SL and sounds qualitatively in agreement with a lower thermal conductivity of SLs.^[7–9]

Another interesting point is related to the comparison of the SET speed of the two materials by a quenching-time characterization. In this experiment, the cell is delivered a pulse train with a constant current amplitude (in the 1–1.5 mA range for bulk GST and in the 0.4–0.5 mA range for SL to match the RESET current amplitude) and a gradually increasing quenching time, from $t_Q = 10 \text{ ns}$ (RESET pulse) to $t_Q = 0.4 \mu\text{s}$ (already in the SET range for bulk GST). The expected behavior of conventional PCM is reported in a resistance-quenching-time (RTQ) plot starting from the RESET state resistance and gradually converging to the SET state resistance according to the involved crystallization kinetics: the relative comparison between bulk GST and SL would be expected to reveal further properties of the SL stack itself. Instead, **Figure 4** reports the RTQ plot with a quite aligned behavior in terms of SET speed between bulk GST and SL, in both transition shape and timing. Such experiment further supports that crystallization in bulk GST and SL is likely dominated by the same phenomenon, i.e., a thermally driven nucleation/growth of nuclei,^[31] as in conventional PCM, thus

Figure 4. SET behavior comparison between bulk GST and SL: very similar plots are shown, revealing a likely similar crystallization kinetics from an amorphous phase. The setup limitation line represents the minimum quenching time allowed by the setup, given the electrical R - C constant experienced by the load path.

strongly supporting the presence of an amorphous phase as the starting point of this experiment in both stacks. In case of one-dimensional displacement of atoms,^[10] stacking faults motion in SL^[19] or other non-thermal frameworks, a significantly different transition should have been expected in terms of shape and timing.

Gathering all the electrical analyses together, a picture has emerged that shows that the SL based devices with GeTe/Sb₂Te₃ phase intermixing, work in a similar fashion as conventional PCM-based devices do. However, they benefit from two key improvements over conventional GST: an increased resistance at the RESET level as a result of a limited segregation within the GST stripes of SL, and a higher thermal resistance than bulk GST, as a result of multiple interfaces and vdW gaps. The obtained results are qualitatively in agreement with some theoretical and experimental studies done on SL stacks that claim a lower thermal conductivity for SLs with respect to bulk GST.^[7–9] Among the electrical evidences reported here, the SET speed characterization represents one of the key points to support the thermal picture: crystallization kinetics requires time and temperature for the nucleation/growth of nuclei within the amorphous phase and a non-thermal picture for SLs would have led to major differences in the RTQ plots. This approach thus relaxes the need to reduce the dimensions of the memory cells aiming at a reduced power consumption. This is especially advantageous for embedded non-volatile memory applications that normally are not fabricated with the state of the art lithography. Furthermore, this approach could make possible to use materials with a higher melting and crystallization temperature and thus improving thermal stability of devices, while retaining acceptable power consumption. However, the major drawback of such cell stack is its weakness against high current amplitudes: the programming current needs to be carefully limited during the early programming cycles to avoid the SL melting and its partial/total breakdown and loss of the I_{PROG} reduction capability due to the overall mixing of the stacked layers, leading to a bulk-like GST operation. Also, the

cycling lifetime, not investigated within this work, needs to be carefully addressed thanks to dedicated algorithms able to keep the programming current evolution through cycles under control and avoid SL damage. However, if SL is operated in the proper conditions, the presumed increased thermal resistance and the accompanying reduction of I_{PROG} make these materials interesting for future use in high density memory arrays. The use of SL in PCM device thus could offer an additional degree of freedom for device optimization and further improvements of device functionality could be expected by fully exploiting the use of SL in PCM device.

Experimental Section

SL-based phase change memory cells were fabricated by depositing alternating layers of GeTe (1 nm) and Sb₂Te₃ (4 nm) on amorphous devices structures having a 2500 nm² bottom contact area or amorphous substrates. Details about the device structure can be found in a previous publication.^[21] The deposition was performed by MBE and monitored by in situ RHEED as described in detail elsewhere.^[16,18] GST reference devices were also fabricated by MBE.^[21] SEM characterization of the device structures was performed using a Hitachi S4800. X-ray diffraction was performed with a PANalytical X'Pert Pro using Cu K α_1 radiation ($\lambda = 1.540598$ Å). The electrical characterization was done using an Agilent 81110 pulse generator to deliver fast programming pulses to the cell and a Le Croy 9350A scope to measure the voltage drop over the device in the pulse time domain to obtain the cell programming current and voltage. A Keithley 236 parameter analyzer was employed to take the readout of the programmed state in the DC regime, in an automatically switched AC/DC circuit. Additional electrical characterization was performed using a Keithley 4200 SCS equipped with a Keithley 4225 pulsed measuring unit. Cross-sectional TEM specimen of SL grown on plain amorphous substrates were prepared by mechanical grinding and ion-polishing with a Gatan PIPS II. High-Resolution TEM (HR-TEM) was performed using a JEOL 2010F.

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Conflict of Interest

The authors declare no conflict of interest.

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non-volatile memories, phase change materials, superlattices

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