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High charge density and mobility in poly(3-hexylthiophene) using a polarizable gate dielectric

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Abstract

Organic field-effect transistors (OFETs) typically exhibit either a high charge transport mobility or a high charge density. Here we demonstrate an OFET in which both the mobility and the charge density have high values of 0.1 cm²/V s and 28 mC/m², respectively. The high charge density is induced by the ferroelectric polarization of the gate dielectric poly(vinylidene fluoride/trifluoroethylene). The high mobility is achieved in a regioregular poly(3-hexylthiophene) semiconductor using a transistor with a top-gate layout that inherently exhibits a smooth semiconductor–dielectric interface. The combination of high mobility and charge density yields a record conductance value for polymer-based FETs of 0.3 μS.

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1. Introduction

Organic field-effect transistors (OFETs) have reached a technological level where they might be applied in a number of products, ranging from RFID tags to active-matrix (AM) driven displays. Active-matrix electronic-paper displays driven by OFETs have recently been demonstrated [1], and application of OFETs for AM liquid crystal displays is also considered. An inherent disadvantage of organic FETs is that the current driving capability is limited by the relatively low mobility, as compared to their inorganic counterparts. A high current response/conductance is advantageous for driving organic light-emitting diodes (OLEDs) and it reduces the charging time of gate capacitors in integrated circuits. The conductance is determined by the product of charge carrier density in the channel, governed by the capacitance of the gate dielectric, and the charge carrier mobility. In a recent demonstration of an AM driven OLED display pentacene-based drive transistors were used, exhibiting a conductance of typically 0.2 μS [2]. These pentacene FETs make use of the high carrier mobility of 0.6 cm²/V s that can be achieved in...
vacuum-deposited small molecules. An important question is whether such a large conductance can also be achieved in solution-processed polymer transistors, of which the mobility is at least an order of magnitude lower as compared to their small-molecule based counterparts. For this a large carrier density and carrier mobility needs to be combined in one single polymer transistor.

One way to increase the maximum charge carrier density is by increasing the capacitance of the gate dielectric. It has been shown that the high capacitance of a polymer electrolyte can induce a charge density of 3 C/m² [3], but only in combination with a strongly limited carrier mobility of 4 × 10⁻⁴ cm²/V s in pentacene, which results in a low conductance value of 0.07 µS. Another approach is to use a thin polymer film with a high dielectric constant \( k \) [4]. One promising candidate material is polyvinylidene fluoride (PVDF) and its co- and terpolymers because it has a high dielectric constant and dielectric strength [5]. A pentacene-based transistor using a PVDF terpolymer gate dielectric with a mobility of 1 cm²/V s has been demonstrated [6]. However, the transistor was made with a low-\( k \) buffer layer on top of the dielectric which lowered the effective \( k \)-value by 50%. The buffer layer was necessary because of the high surface roughness of the dielectric layer, which would have lowered the mobility due to charge trapping effects inside roughness valleys at the dielectric–semiconductor interface [7]. Field-effect transistors based on pentacene and regioregular poly(3-hexylthiophene) (rr-P3HT) with a PVDF gate dielectric without a buffer layer have also been demonstrated [8,9]. The highest mobility was 8 × 10⁻³ cm²/V s in rr-P3HT, which was obtained using a PVDF gate dielectric with a surface roughness of 5 nm [9]. In recent literature the reported mobility of rr-P3HT is most often higher than 1 × 10⁻² cm²/V s [10]. The fact that the mobility of rr-P3HT is generally higher confirms that the mobility on PVDF without a buffer layer is limited by the surface roughness of PVDF. In this manuscript we demonstrate that a top-gate transistor layout enables a smooth interface between rr-P3HT and PVDF copolymer poly(vinylidene fluoride/trifluoroethylene) (P(VDF-TrFE)). The change from a bottom-gate to a top-gate layout is a more expedient solution to the roughness problem than using a buffer layer, because it does not lower the effective \( k \)-value of the gate dielectric. With the top-gate transistor layout a semiconductor mobility of 0.1 cm²/V s is obtained in rr-P3HT, which is an increase of about one order of magnitude. Furthermore, we demonstrate that a charge density of 28 mC/m² is induced by the ferroelectric and dielectric polarization of P(VDF-TrFE). The combination of high mobility and charge density induces a large conductance of 0.3 µS. It is this large conductance value that makes the transistors applicable as drive transistors in active-matrix OLED displays [2,11].

2. Experimental

The top-gate field-effect transistor layout is shown in Fig. 1(a), with silver source, drain and gate electrodes and a P(VDF-TrFE) gate dielectric film on top of the rr-P3HT semiconductor film. The transistors were prepared upon clean glass substrates onto which silver source–drain electrodes were deposited with shadow mask evaporation, using a wire to create the channel. The substrates were subsequently annealed at 140 °C in air to increase the adhesion. The workfunction of the annealed silver measured with a Kelvin probe was 4.4 eV. Regioregular poly(3-hexylthiophene) (electronic grade; 98.5% regioregular; Rieke Metals, Inc.) was purified as described in a previous report [9]. Chloroform solutions were spin coated in a N₂ filled glovebox. A rotation speed of 4000 rpm was used to minimize the surface roughness. The layer
thickness was typically 60 nm. The samples were subsequently annealed in a vacuum oven at 140 °C to enhance the crystallinity of the rr-P3HT. The topography of an annealed rr-P3HT layer as measured with an AFM is presented in Fig. 1(b). The root-mean-square roughness derived is about 0.7 nm. On top of this layer, the gate dielectric was applied by spin coating filtered 2-butanone solutions of either poly(trifluoroethylene) (PTrFE) or poly(vinylidene fluoride-trifluoroethylene) 65–35 mol% random copolymer (Solvay, Belgium). It is crucial in this step that the semiconductor layer does not dissolve in the solvent 2-butanone. A solubility test showed no coloration of this colorless solvent after prolonged stirring, indicating that 2-butanone is a non-solvent to rr-P3HT. The samples were annealed again in a vacuum oven at 138 °C to enhance the crystallinity of the gate dielectric. The transistors were finalized by evaporation of silver gate electrodes. Current transport measurements were performed in dark and vacuum using a Keithley 4200 semiconductor analyzer. Polymer layer thicknesses were determined using a Dektak profilometer.

3. Results and discussion

Fig. 2 shows a typical transfer curve measurement of a top-gate ferroelectric FET (FeFET) as depicted in Fig. 1(a). The drain current has a bistability at zero gate bias due to the ferroelectric polarization of the gate dielectric, similar to the results obtained for FeFETs with a bottom-gate layout and a poly(p-phenylene vinylene) derivative as the semiconductor [12]. The charge transport mobility value derived from the drain current slope in the on-state at zero gate bias is 0.12 cm²/V s. We can compare this mobility value to the results obtained by us with rr-P3HT bottom-gate FeFETs because all the active materials used were identical [9]. The mobility for the bottom-gate FeFETs was $8 \times 10^{-3}$ cm²/V s which shows that changing the transistor layout from a bottom-gate to a top-gate geometry increases the mobility by more than one order of magnitude. The mobility increase can be explained by the semiconductor interface roughness of the transistors. For the bottom-gate transistors, this roughness is determined by the surface roughness of 5 nm of P(VDF-TrFE), but for the top-gate transistors it is determined by the roughness of 0.7 nm of rr-P3HT. The surface roughness of the bottom layers determine the semiconductor interface roughness, because the bottom layers are insoluble in the solvents used for depositing the second layer (see Section 2).

In Fig. 3, the induced charge density in the FeFET is estimated by comparing the current response of non-ferroelectric with ferroelectric FETs. The non-ferroelectric FETs were prepared...
in an identical way to the FeFETs, but with polytri-
fluoroethylene (PTrFE) as the gate dielectric. 

PTrFE is a highly polar fluoropolymer with the 
same dielectric constant as P(VDF-TrFE), but it 
has a negligible ferroelectric polarization [12]. 

In this way, an estimate of 20 mC/m² is obtained for 
the induced charge in the FeFET at zero gate bias. 

This value is consistent with a previous value of 
18 mC/m² found for FeFETs with a poly(p-phenyl-
eine vinylene) derivative as the semiconductor [12]. 

At a gate voltage of $V_G = -150$ V the induced charge 
increases to 28 mC/m². This induced surface charge 
density is a high value compared to what can be 
obtained with conventional Si⁺⁺/SiO₂ transistors, 
because these transistors are limited by the dielectric 
breakdown of SiO₂ at high applied fields [12]. The 
maximum conductance in Fig. 3 is 0.3 μS which to 
our knowledge is the largest value ever reported 
for a semiconducting polymer. The large conduc-
tance is a consequence of the high semiconductor 
mobility and induced charge density because it is 
the product of these two.

Having determined the charge density in the 
FeFET, we can confirm the linear mobility value 
using the current–voltage characteristics of the 
FeFET and

$$I_D = \frac{W}{L} \mu C_i (V_G - V_T) V_D,$$  \hspace{1cm} (1)

which is the standard equation for a FET operating 
in the linear regime [13]. We can neglect the thresh-
old voltage in Eq. (1) because the effective gate volt-
age, that consists of an applied gate voltage and the 
erroelectric polarization, is high. If we also replace 
the product of $V_G$ and $C_i$ by the induced charge 
density $\rho$ we obtain

$$I_D = \frac{W}{L} \mu \rho V_D.$$  \hspace{1cm} (2)

Fig. 4 presents the current–voltage characteristic 
of the FeFETs at a gate voltage of $V_G = -100$ V, operating 
in the linear regime. Using a $\rho$ value of 25 mC/
m², extracted from Fig. 3 for a gate voltage of 
$V_G = -100$ V, we obtain a good fit with Eq. (2) for a 
 mobility value of 0.15 cm²/V s. This value confirms 
the mobility value derived from Fig. 2. Fig. 4 also 
demonstrates the high current response of the tran-
sistor in the milliamp regime that enables it to drive 
organic light-emitting diodes. For practical applica-
tions the gate voltage of $V_G = -100$ V would need to be 
reduced by using a thinner gate dielectric. FeFETs 
with a gate dielectric thickness of 200 nm have been 
demonstrated [9], which would reduce the gate volt-
age from $-100$ V to $-11$ V.

An increase of the $k$-value of the gate dielectric 
generally leads to a sharp decrease of the mobility of 
organic semiconductors [14]. This decrease is 
due to the dipolar disorder inside polar dielectrics 
which broadens the density of states and ultimately 
increases the energy barrier for hopping transport. 

The highest mobility reported for rr-P3HT is 
0.3 cm²/V s [15]. Considering the $k$-value of 
P(VDF-TrFE) of 11 and the dependence of the 
 mobility on the $k$-value of the gate dielectric, a max-
imum semiconductor mobility of 0.03 cm²/V s is 
extpected for a FeFET. This is about one order of 
magnitude lower than the observed mobility of 
0.1 cm²/V s in the FeFET. However, the charge 
density in the FeFET has a high value and the 
 mobility of most organic semiconductors increases 
with the charge density [16]. The high charge density 
can therefore explain the high mobility in the 
FeFET.

We note that a recent report demonstrated a 
transistor that is similar to the one presented here 
[17]. However, the measurement results are dissimi-
lar to the present results: the rr-P3HT charge trans-
port mobility and the maximum conductance had 
low values of $3.4 \times 10^{-3}$ cm²/V s and 9 nS, respec-
tively; the gate bias attenuates the drain current by 
a factor of 2.5, while the on/off ratio in Fig. 2 is 
$10^4$; the gate insulator leakage current was 
200 mA/m² ($=2 \times 10^{-5}$ A/cm²) at an applied field 
of 25 MV/m ($=250$ kV/cm), which is 100 times
higher than our result of 2 mA/m$^2$ at an applied field of 90 MV/m [9]. The lower performance suggests an adverse effect caused by a suboptimal device processing.

4. Conclusions

We have shown that the mobility of a transistor with rr-P3HT as the semiconductor and P(VDF-TrFE) as the gate dielectric was increased by an order of magnitude to 0.1 cm$^2$/V s by using a top-gate transistor layout, because this reduces the semiconductor–dielectric interface roughness from 5 to 0.7 nm. A high charge density of 28 mC/m$^2$ was induced by the polarizable gate dielectric which led to a record conductance value for polymer FETs of 0.3 $\mu$S.

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